ACHARYA INSTITUTE OF TECHNOLOGY,

Bangalore

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

NOTES FOR

"BASIC ELECTRONICS"

(18ELN14/24)

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SEMICONDUCTOR DIODES AND APPLICATIONS.

Introduction: The term diode identifies a two-electrode & two-terminal device. & A Diode is a two-layer (PN junction) device which facilitates conduction in one direction and blocks conduction in other direction. Diode offers a low resistance when fdward biased and behaves as a open ckt when reverse biased. A constant voltage drop occurs across the diode when the diode is fdward biased.

PN-Junction

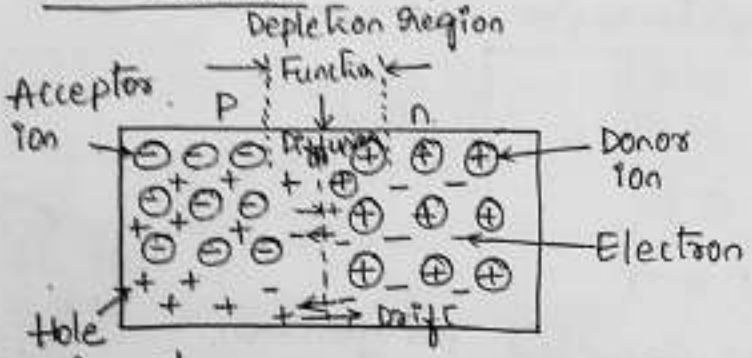

fig: phenomenon at PN-junction.

As shown in fig, PN junction is formed when thin layers of p and N-type semiconductors are joined together that results in the following phenomenon.

* The majority holes from p-side diffuse into N-side and vice versa.
* Recombination of electrons and holes in a narrow region on both sides of the junction results in uncovered fixed positive ions on N-side and fixed negative ions on p-sides.
* This is the Depletion region where no free electron and holes present.

* The electric field set up by the positive and negative ions prevents further flow of electrons and holes.
* The electric field causes the movement of minority carriers in opposite direction that provides a minority carrier drift current.
* In steady state there is no net current flow across the junction.

The simplified diagram of an open circuit PN junction diode as shown in fig below, where V_0 is the constant potential. The p-side terminal is called anode and the N-side terminal is the cathode.

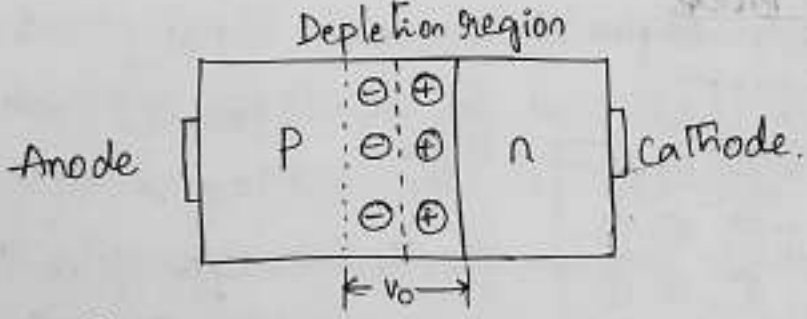

fig: An open circuited PN Junction.

PN-Junction Diode:

PN Junction Diode has a ability to permit a current flow when it forward biased and it blocks the current flow when it is reverse biased hence it can be used as the "Switch".

The Switch is said to be 'ON' when it is forward biased and 'OFF' when it is reverse biased. It is provided with the copper wire connecting leads becomes an electronic device known as a Diode.

The circuit symbol of PN-junction diode and ckt symbol in the fig below.

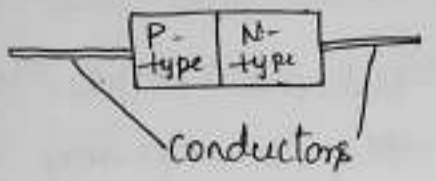

fig: PN Junction Diode.

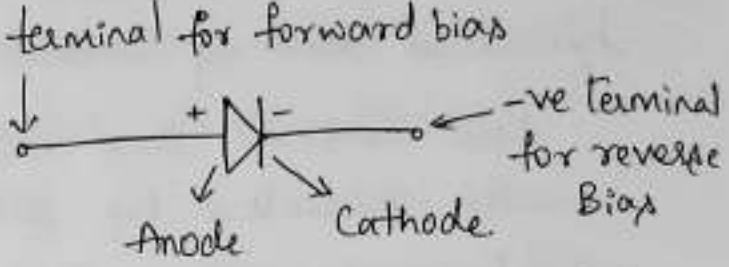

fig: Diode circuit symbol.

The circuit symbol of a diode is an arrowhead and a bar. The arrowhead indicates the flow directions of the current when it is forward biased.

A PN Junction diode can be destroyed by a high level of forward current overheating the device. It can also destroyed by a large reverse voltage causing the junction to breakdown. In general, physically large diodes pass the largest currents and survive the largest reverse voltages. We can classify PN junction diodes as low current, medium current and High current Diodes.

The low current device may be of size 0.3cm long, the cathode is usually denoted by a coloured band, and is capable of passing a maximum current of 100mA (75V).

The medium current diode can pass a forward current of about 400mA and survive over 200V. of reverse voltage. The anode and cathode terminals are indicated by a diode symbol on the side of the Diode.

High current diodes & power diodes can pass forward currents of many amperes and can survive several hundred volts of reverse bias.

Low current and medium current diodes are usually mounted by soldering the connecting leads to terminals. Power dissipated in the device is carried away by air convection and by heat conduction along the connecting leads. Air convection is inadequate in power diodes hence these diodes are designed for mechanically connecting to metal heat sink.

Biasing: Applying External voltage to any electronic component is called Biasing. PN Junction can be operated in three modes.

1) unbiased PN Junction
2) forward Biased PN Junction
3) Reverse Biased PN Junction.

Forward Biasing of PN Junction | Forward characteristics of PN Junction.

A positive bias vlg is applied to the p-side and the negative bias vlg is applied to the N-side of the PN Junction is called Forward Biasing.

In P-side holes are the majority carriers and in the N-side electrons are the majority carriers. As the holes on the P-side are +vely charged particles they are repelled from the positive bias voltage.

Forward characteristics is plot of forward voltage (V_F) versus forward current (I_F). From these curves we see that the little forward current flows until V_F exceeds the junction barrier potential 0.3 for Ge and 0.7 for Si

With the increase in V_F towards the knee characteristics. the barrier potential gradually reduced. Beyond the knee voltage the barrier voltage is fully overcome and I_F increases with increases in V_F and thus this behaviour of blocking is termed as resistance. The forward biased PN junction is said to be provide low resistance.

Forward Resistance (at point q) for silicon.

$$R_f = \frac{0.7V}{20mA} = 35 ohms.$$

Forward resistance (at point p) for Germanium.

$$R_f = \frac{0.3V}{20mA} = 15 ohms.$$

R_f is not used in practise. r_d, the ac resistance & the dynamic resistance of the junction is used. And it can be calculated as

$$r_d = \frac{1}{\text{slope of forward characteristic beyond the knee voltage}}$$

i.e $r_d = \dfrac{1}{\frac{\Delta I_F}{\Delta V_F}}$

$$\boxed{r_d = \frac{\Delta V_F}{\Delta I_F}}$$

and are forced to move towards the junction. Similarly the electrons on N-side are repelled by the application of the -ve bias voltage and are move towards the junction. Due to this the depletion region is narrower down. and also the barrier potential is reduced as shown in fig ②.

As the applied voltage is increased from '0' the barrier potential gets gradually too small and becomes disappeared and the charge carriers readily move from P to N and N to P freely Thus the current flows and the junction is forward biased

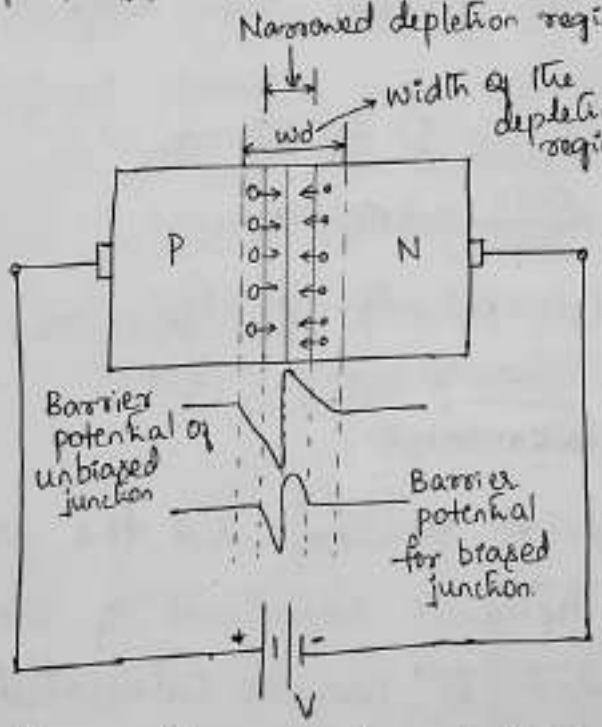

fig ②: forward Biased PN Junction.

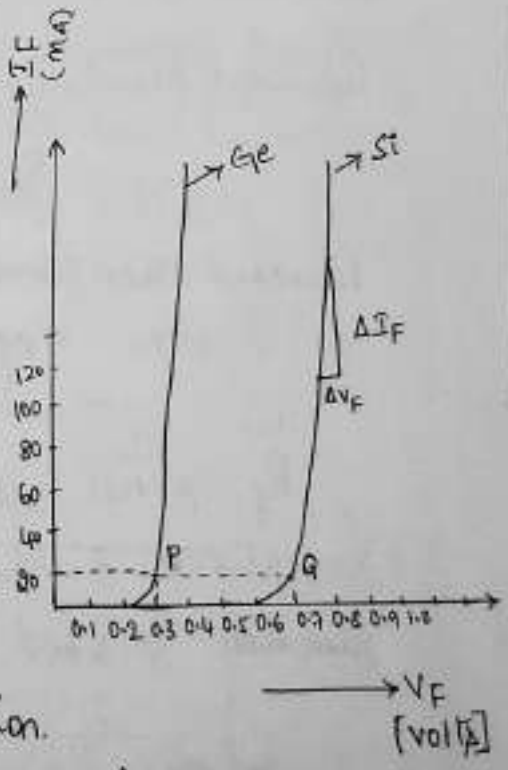

fig ③: forward characteristics of PN Junction.

The forward characteristics of a PN junction are as shown in fig ③, for the silicon and Germanium semiconductors

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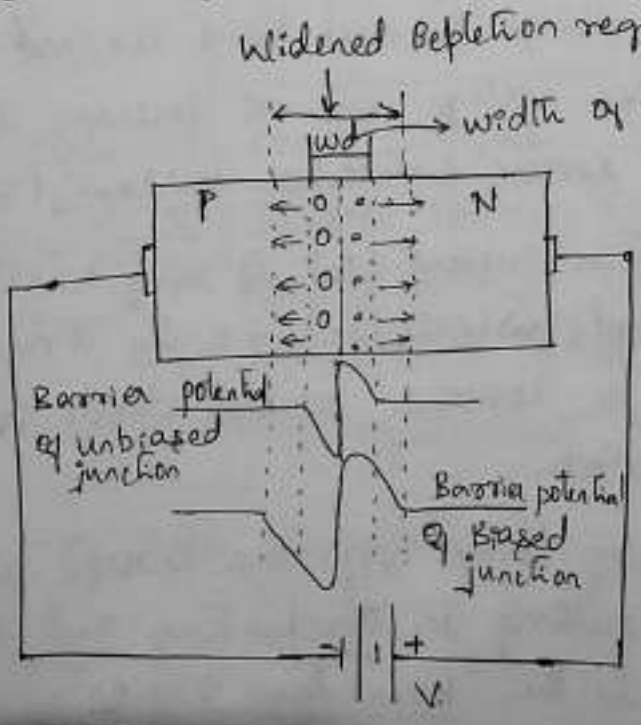
$$\boxed{r_d = \frac{\Delta V_F}{\Delta I_F}}$$

Reverse Biasing of pN Junction / Reverse characteristic of pN Junction

A positive bias vlg is applied to the N-side and the negative bias vlg is applied to the p-side of the pN Junction is called Reverse Biasing.

On application of an external bias i-e +ve vlg to the N-side and -ve to the p-side. Electrons from the N-side are attracted to the bias terminal and holes from the p-side are attracted to the -ve terminal. As a result of this, the depletion region is widened and the barrier potential is increased by the magnitude of the applied voltage. Due to the increase in barrier potential and the resultant electric field. it is not possible for the majority current to flow across the junction. and the junction is said to be reverse biased as shown in fig ③.



fig③: Reverse Biased PN Junction.

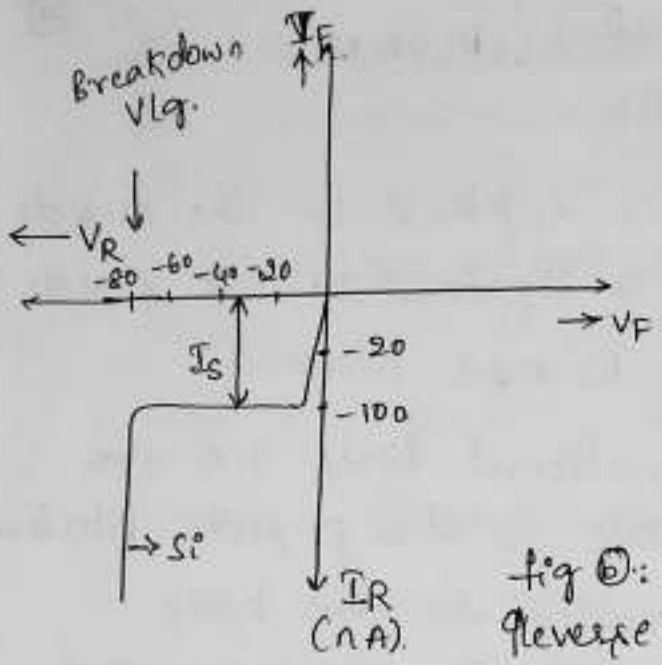


fig ⓑ: Reverse characteristic of Silicon

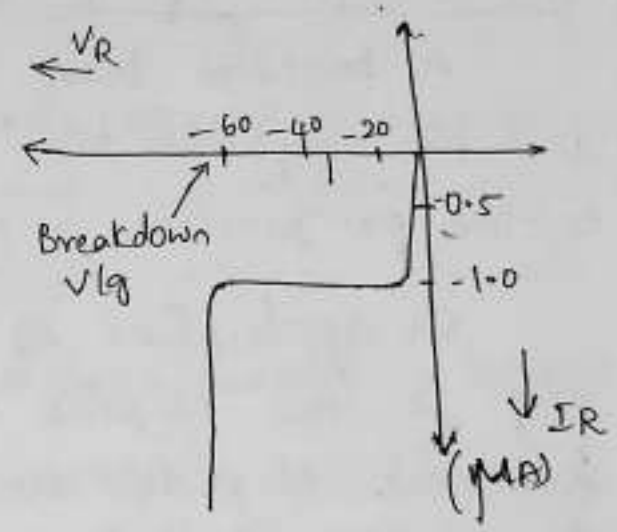


fig ⓒ: forward characteristic of Germanium.

Reverse Bias characteristic is the plot of Reverse voltage (V_R) versus Reverse current (I_R). Reverse Bias Characteristics for Si and Ge is ashown in fig ⓑ & ⓒ respectively.

A Small reverse bias voltage is enough to pull across the available minority carriers across the junction. When all the minority charge carriers have crossed over, further increase in bias voltage will not increase the current. This is called Reverse saturation current (I_S).

The Reverse saturation current (I_S) is very much smaller than the forward current (I_F). i.e I_S is negligible compared to I_F. Hence a reverse biased diode may be considered as open switch.

At particular value of Reverse vlg, the reverse current suddenly shoots up, resulting in overheating and the diode is said to be in the "Breakdown region"

The breakdown voltage for silicon PN junction is about 80V and for germanium PN junction is about 60V as shown in fig (b) and (c).

From the reverse characteristics, we can find the Reverse resistance as below.

for Si, $V_R = 50V$, $I_S = 100nA$

$\therefore$ Reverse resistance, $R_R = \frac{V_R}{I_S} = \frac{50V}{100nA} = 500M\Omega$

The reverse characteristics of a Germanium diode are similar to that of a silicon diode, except the saturation current. In case of Ge diode, the saturation current at room temperature (95°C) is around 1.0mA which exceeds the Reverse current.

Reverse resistance, $R_R = \frac{V_R}{I_S} = \frac{50V}{1MA} = 50M\Omega$.

The Diode Current Equation:

The General characteristics of the PN junction are defined by the following Diode current Equation.

$$\boxed{I = I_o \left[e^{\frac{V}{\eta V_T}} - 1 \right]}$$

where, I = Diode current

I_o = Reverse Saturation current

V = Appled voltage

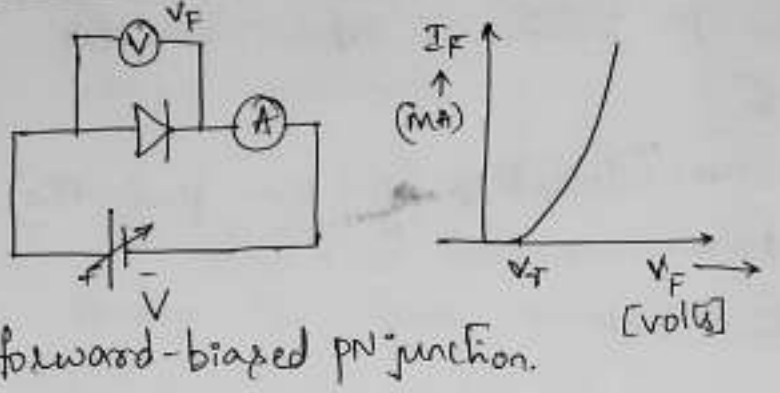
η = Constant : $\eta = 2$ for Si, $\eta = 1$ for Ge.

V_T = volt equivalent of temperature = $\frac{T}{11600}$

At room temperature $T = 300°K$ $\therefore V_T = \frac{300°K}{11600}$

$$\boxed{V_T = 26mV}$$

Diode Current Equation for Forward Bias



forward-biased PN junction.

The Diode-Current equation is.

$$I = I_0 \left[e^{\frac{V}{\eta V_T}} - 1 \right]$$

when the Diode is forward biased V is +ve, and $I = I_F$. when $V \gg V_T$. then $e^{V/\eta V_T} \gg 1$. then the above equation is reduced to

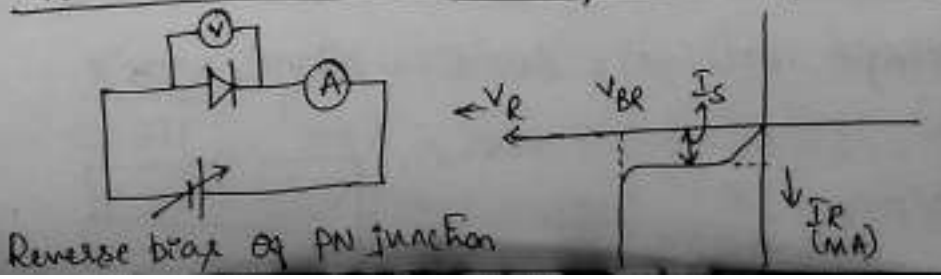
$$I = I_0 e^{\frac{V}{\eta V_T}}$$

→ This equation shows that the diode current rises exponentially when the diode is forward biased as shown in the fig above.

From the forward characteristics it is observed that forward current is zero upto a certain forward vlg V_γ. This vlg is called as "cut-in voltage". It is the vlg at which the diode start conducting. As the voltage is increased beyond the cut-in vlg V_γ. the current increases rapidly. The cut-in vlg is sometimes called "offset vlg" or "break point vlg" or threshold vlg.

cut-in vlg differs for different semiconductor material and different method of fabrication. At room temperature, the cut-in vlg for Ge is 0.2 and for silicon it is about 0.6V.

The Diode Current Equation for Reverse Bias.



Reverse bias of PN junction

Variable reverse bias voltage is applied across the pN junction diode as shown in fig. The Diode current equation is

$$I = I_0 \left[e^{\frac{V}{\eta V_T}} - 1 \right]$$

When the reverse or negative vlg is applied across the diode. V is negative and $I = I_R$ and when $V \gg V_T$

$$e^{-V/\eta V_T} = \frac{1}{e^{V/\eta V_T}} \ll 1$$

Hence, the above current diode equation reduces to

$$\boxed{I_R = -I_0}$$

The above equation shows that the current is constant and is independent of the applied reverse bias. When the Reverse vlg is increased to V_{RB}, breakdown occurs.

Note: The Diode current equation is not applicable during Breakdown.

Examples:

1) For a silicon diode at a working temperature of 25°C the forward voltage applied across the diode is 0.5V. Determine its forward current if the reverse saturation current is 10nA.

Soln: Forward current, $I_F = I_0 \left[e^{\frac{V}{\eta V_T}} - 1 \right]$

Given: I_0 = Reverse saturation current = 10nA = 10×10^{-9} A.

V = forward voltage across the diode = 0.5V

T = 25°C = 25 + 273 = 298°K.

$\therefore V_T = \frac{T^\circ}{11600} = \frac{298}{11600} = 25.68$mV.

$\eta = 2$ for silicon.

$$I_F = 10\times10^{-9}\left[e^{\frac{0.5}{2\times2.5\times10^{-3}}} - 1\right]$$

$$\boxed{I_F = 0.169\,mA}$$

2) A Germanium diode draws 40mA with a forward bias of 0.25V. The junction is at room temperature of 293K Calculate the Reverse saturation current. Take $\eta = 1$

Soln: Given: $I_F = 40mA$

$V = 0.25V$

$T = 293\,K$

$\eta = 1$

$$V_T = \frac{293}{11600} = 0.025$$

$$I_F = I_0\left[e^{\frac{V}{\eta V_T}} - 1\right]$$

$$I_0 = \frac{I_F}{e^{V/\eta V_T} - 1}$$

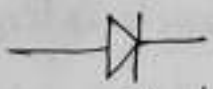
$$= \frac{40\times10^{-3}}{e^{0.25/1\times25\times10^{-3}} - 1}$$

$$\boxed{I_0 = 1.82\,\mu A}$$

Ideal Diode Characteristics: [Ideal Diode Approximation]

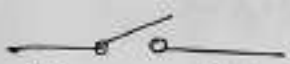
An ideal diode is one which has following characteristics

1) The cut-in voltage is zero, since there is no barrier potential. any small forward bias voltage causes conduction through the devices.
2) The forward resistance is zero.
3) The reverse resistance is infinity
4) The Diode readily conducts when it is forward biased and it blocks conduction when it is reverse biased The reverse saturation current is zero.



Ideal diode

forward biased



Reverse biased

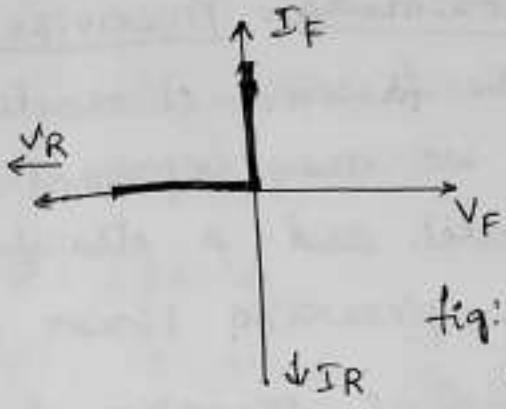


fig: Ideal Diode characteristics.

An ideal diode acts as a switch. An ordinary switch has zero resistance when it is closed and infinite resistance when it is open. The switch is said to be close when it is ~~forward~~ biased and switch is said to be open when it is reverse biased.

Diode Approximations.

In practice an ideal diode does not exist, there are many applications where diodes can be assumed to be near ideal devices.

Second Approximation:

Diodes are assumed to be nearly ideal for situations which require exact values of load current and load vlg but ideal diodes does not exist in practical situations. Hence we assume the second approximation model. In this we consider vlg drop of silicon 0.7V and Germanium as 0.3V. Constant vlg source of 0.7V & 0.3V is assumed to be in series with Ideal diode as shown in fig.

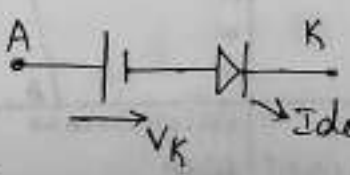
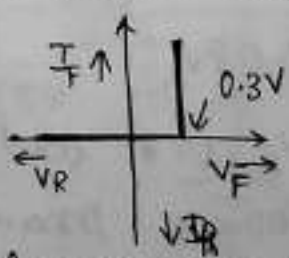


fig: Second approximation.



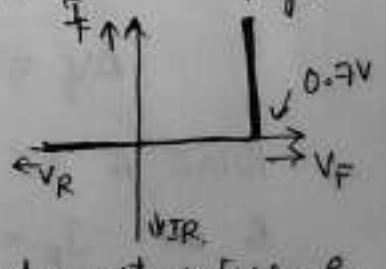


fig: Approximate characteristics for Ge & Si

Third Approximation: Piecewise Linear characteristics

when the fdward characteristic of a diode is not available. we may represent the device as a piecewise linear model. and A-straight-line approximation called the piecewise Linear characteristic.

To construct the piecewise linear characteristic, V_F is first marked on the horizontal axis, as shown in fig. then starting at V_F, a straight line is drawn with a slope equal to the diode dynamic resistance.

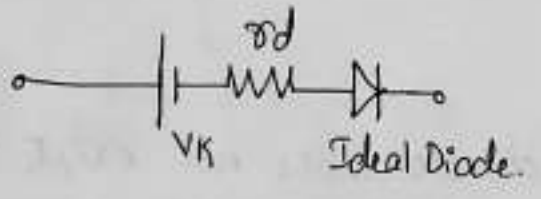


fig: Third Approximation ckt.

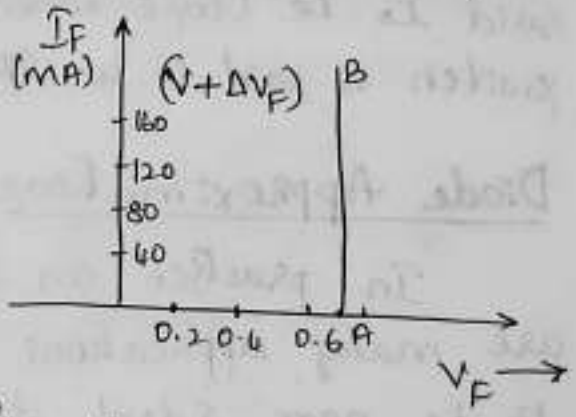


fig: piecewise Linear characteristics of a diode.

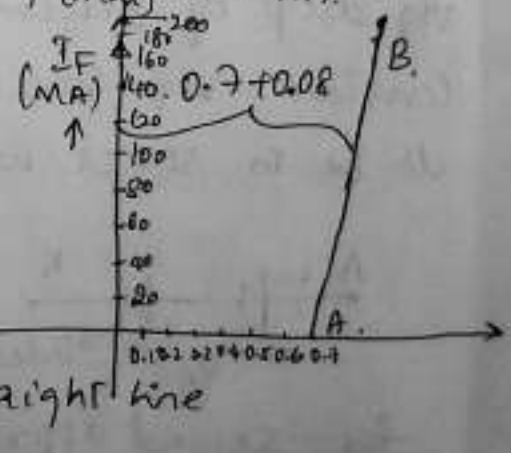
Ex: Construct the piecewise-linear characteristic for a silicon diode that has a 0.4Ω, Dynamic resistance and a 200mA maximum forward current

Given: $V_F = 0.7V$, $r_d = 0.4\Omega$, $I_{F(max)} = 200mA$.

$$\Delta V_F = \Delta I_F \times r_d$$

$$= 200mA \times 0.4$$

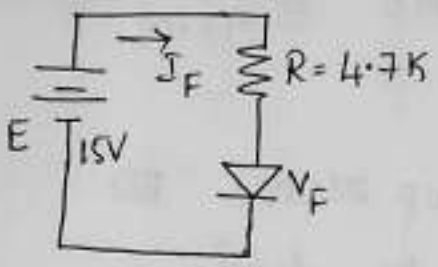
$$\Delta V_F = 0.08V$$



Point A at $V_F = 0.7$. and point B at $I_F = 200mA$. Draw a straight line with slope rd. from B to A.

Examples:

1) A Silicon diode is used in the circuit as shown in fig. Calculate Diode current.



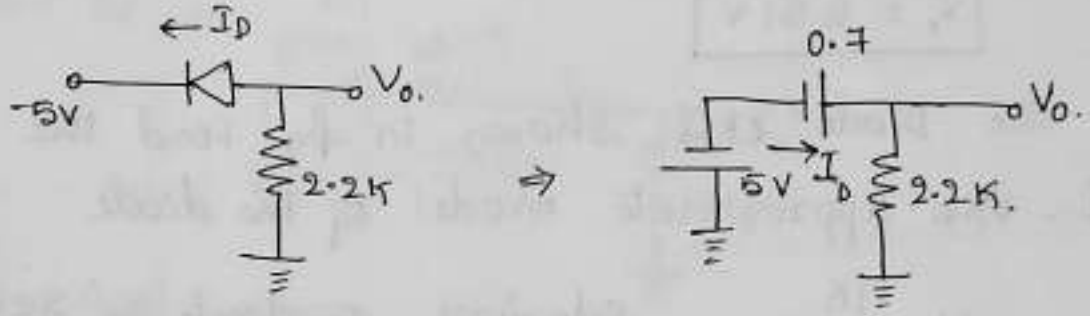
$$E = I_F R + V_F$$

$$I_F = \frac{E - V_F}{R} = \frac{15 - 0.7}{4.7K}$$

$$\boxed{I_F = 3.04mA}$$

2) For the Diode circuit, Determine I_D & V_o using approximation model.

a)



Applying KVL, $5 = 0.7 + 2.2 \times 10^3 \cdot I_D$.

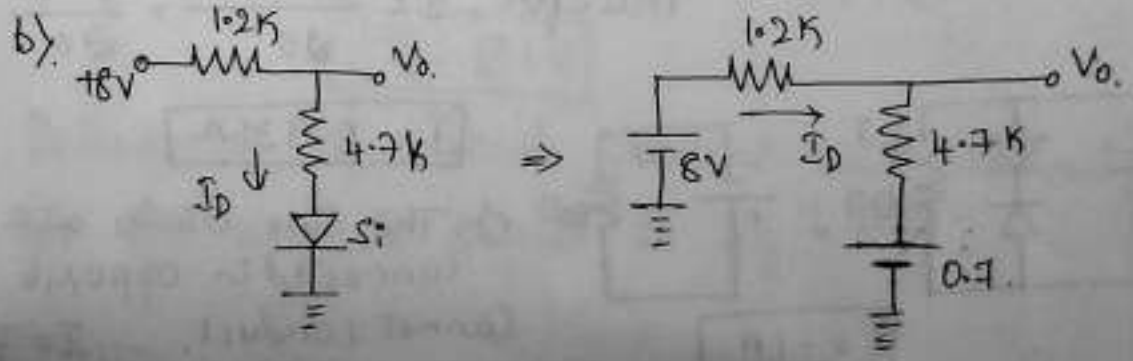
$$I_D = \frac{5 - 0.7}{2.2 \times 10^3} = 1.954mA.$$

V_o is the voltage across the 2.2K resistor.

$$V_o = 2.2 \times 10^3 \times 1.95 \times 10^{-3}$$

$$\boxed{V_o = 4.29V. \simeq 4.3V}$$ or $V_o = 5V - 0.7 = 4.7V.$

b)



Applying KVL, $8V = 1.2K \times I_D + 4.7 \times I_D + 0.7$.

$$8V = I_D (1.2K + 4.7K) + 0.7$$

$$I_D = \frac{8 - 0.7}{(1.2+4.7)\times 10^3} = \frac{7.3}{5.9\times 10^3}$$

$$\boxed{I_D = 1.237\,mA}$$

o/p voltage V_o is the v/g drop across the resistor 4.7 K and drop across the diode.

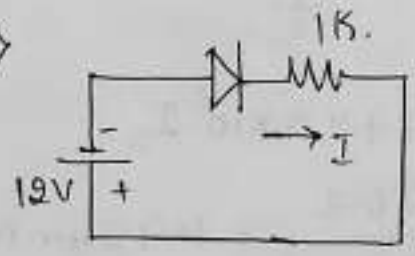
$$V_o = I_D \times 4.7K + 0.7$$

$$= 1.237 \times 10^{-3} \times 4.7 \times 10^3 + 0.7$$

$$\boxed{V_o = 6.51\,V}$$

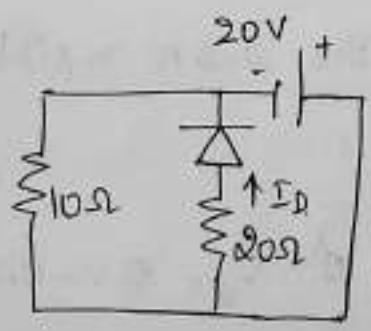
3) For the Diode ckt shown in fig. Find the value of I. Use approximate model of the diode.

a)



Soln a) The Si diode is reverse biased by 12V, so it does not conduct.

b)

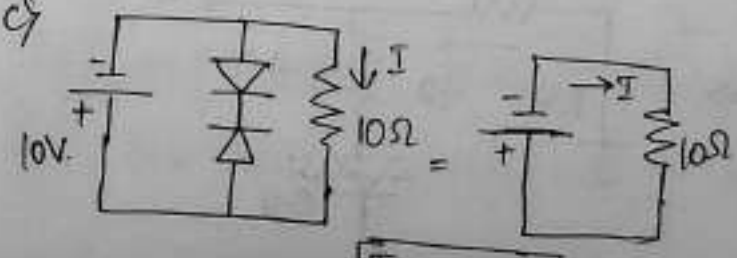


b) The voltage across the diode branch is 20V which is independent of resistor 10Ω.

Therefore, $I = \frac{20 - 0.7}{20} = \frac{19.3}{20}$

$$\boxed{I = 0.936A}$$

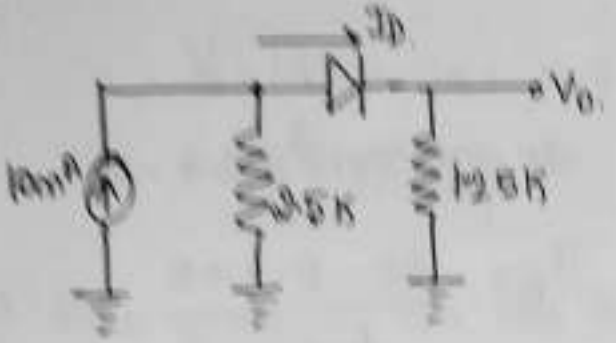
c)



$$\boxed{I = -1A}$$

c) The two diodes are connected in opposite and cannot conduct. $\therefore I = \frac{-10}{10} = -1A$

For the diode ckt shown determine V_0 & I_D.



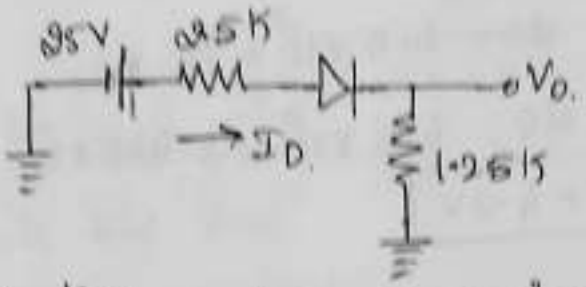
Soln: The given circuit contains current source, convert the current source into voltage source in series with the resistance.

Using ohm's law, $V = IR$

$V = 10\times10^{-3} \times 2.5\times10^{3}$

$\boxed{V = 25V}$

Replacing current source by vlg source the circuit will be ⇒



Applying KVL, $25 = 2.5\times10^{3}\times I_D + 0.7 + 1.25\times10^{3}\times I_D$

$$I_D = \frac{25 - 0.7}{(2.5+1.25)\times10^{3}}$$

$\boxed{I_D = 6.48mA}$

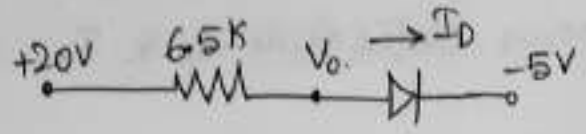
output vlg will be the drop across the resistor 1.25K.

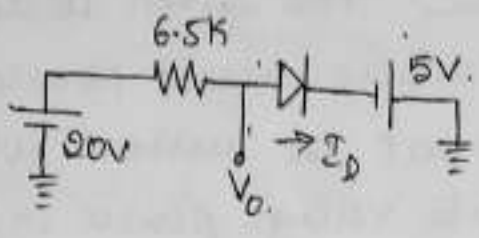
$\therefore V_0 = 1.25K \times I_D$

$= 1.25\times10^{3} \times 6.48\times10^{-3}$

$\boxed{V_0 = 8.1V}$

5) Determine the Diode current and the output vlg. for the circuits shown in fig.

a) 



$$20 = I_D \times 6.5 \times 10^3 + 0.7 - 5$$

$$I_D = \frac{20 - 0.7 + 5}{6.5 \times 10^3}$$

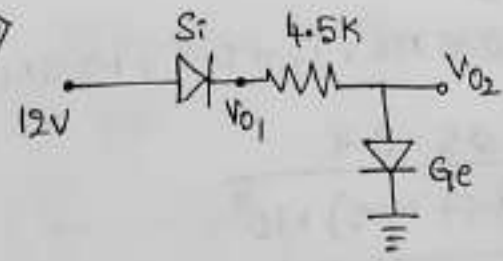
$$\boxed{I_D = 3.738\,mA}$$

O/p voltage V_o is the Difference b/w the appled voltage applied and the v/g drop across the 6.5K.

$$V_o = 20 - 6.5 \times 10^3 \times I_D.$$

$$= 20 - 6.5 \times 10^3 \times 3.738 \times 10^{-3}$$

$$\boxed{V_o = -4.3V.}$$

b) 

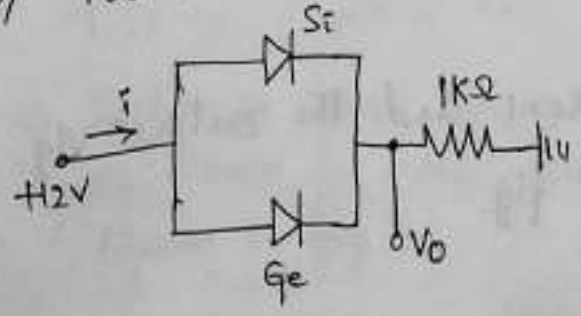
Determine V_{O1} & V_{O2} for the given circuit.

$$V_{O1} = 12 - 0.7 = 11.3V.$$

$\boxed{V_{O2} = 0.3V}$ & $V_T(Ge) = 0.3V$ when conducting.

V_{O2} is the voltage across the Ge diode.

6) For the diode network shown in fig. determine V_o.



The threshold voltage for Si = 0.7 and Ge = 0.3.

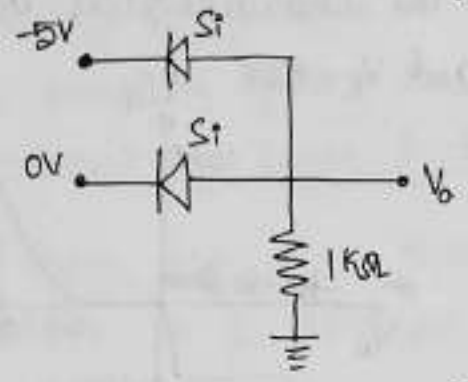
∴ Ge starts conducting before Silicon.

$\therefore \quad I = \frac{12-0.3}{1} = 11.7\,mA.$

$V_0 = 1k\Omega \times 11.7m = 11.7$

$\therefore \boxed{V_0 = 11.7V}$

7) Determine V_0 for the negative logic OR gate.

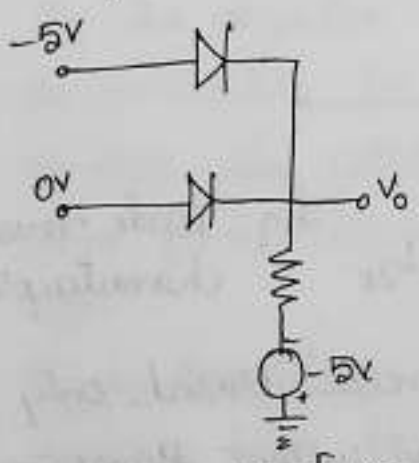


Soln: Only the top diode is connected in forward biased. Hence only top diode conducts.

$\therefore \quad V_0 = -5 - (-0.7) = -4.3V.$

The output will be $V_0 = -4.3V$ (high of negative logic) for input $-5V$ and the output will be zero (low) if the inputs are zero.

8) Determine V_0 for negative logic AND gate as shown in fig.



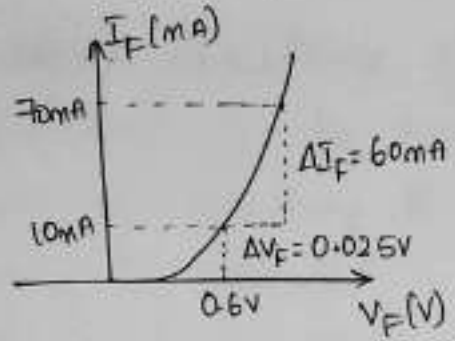
Soln: The lower diode will conduct $V_0 = 0V$.

If both the inputs are 0V, both diodes conduct $V_0 = 0V$ (low, 0). If both inputs are $-5V$, both diodes do not conduct, $V_0 = -5V$ (high, 1)

$-5V$ = high and 0V = low, 0.

This is negative AND.

9) Determine the Dynamic resistance at forward current of 70mA for the diode characteristics given as shown in fig.

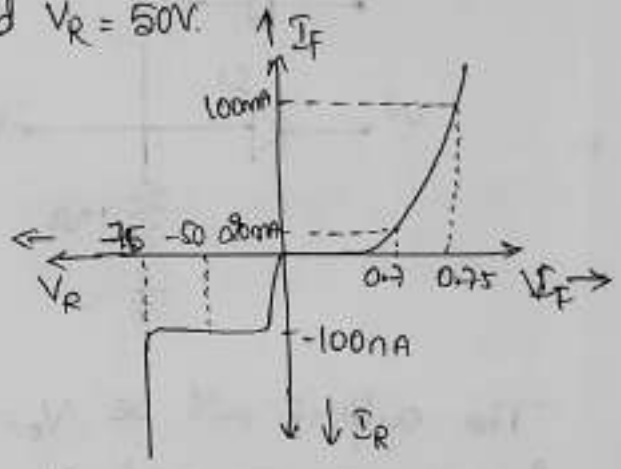


$I_F = 70mA.$

$r_d = \frac{\Delta V_F}{\Delta I_F} = \frac{0.025V}{60m.}$

$\boxed{r_d = 0.42\Omega}$

10) Calculate the forward and reverse resistances offered by a silicon diode with the characteristics as shown in fig. At $I_F = 100mA.$ and $V_R = 50V.$



1) $R_F = \frac{V_F}{I_F} = \frac{0.75}{100mA.} = 7.5\Omega$

2) at $V_R = -50V$, $I_R = -100nA.$

$R_R = \frac{-50V}{-100nA} = 500M\Omega.$

ZENER DIODES.

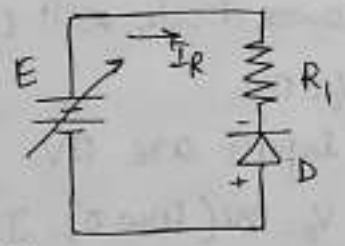


fig: Diode resistor ckt.

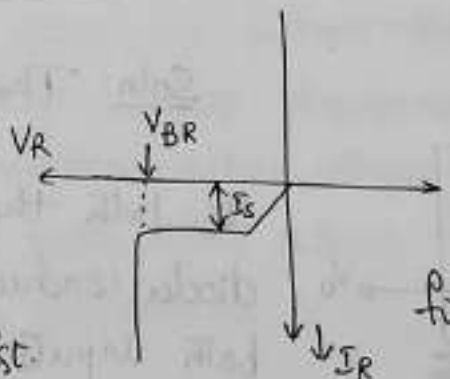


fig: Diode reverse characteristics

When a junction diode is reverse biased, only very small amount of saturation current flows, I_S as shown in the reverse characteristics. When the reverse voltage is increased sufficiently, the junction breaks down and a large reverse current flows. If the reverse current is limited by means of suitable

series resistance, the power dissipation in the junction can be kept constant to a level that will not destroy the device. In this case the diode may be operated in the reverse breakdown. Diodes designed for this operation in reverse breakdown are found to have a breakdown vlg that remains extremely stable over a wide range of current levels. This property gives the breakdown diodes & are also called as Zener Diodes.

There are two mechanisms that cause breakdown in a reverse biased pN junction.

1) Avalanche breakdown.
2) Zener breakdown.

Avalanche Breakdown: when the breakdown voltage is greater than 6V, the electrons in the reverse saturation current can be given enough energy to dislodge other electrons when they strike atoms in the depletion region. This phenomenon is known as ionization by collision. When these electrons freed in this way collide with other atoms they release more free elections, producing a chain or avalanche effect.

Zener Breakdown: When a diode is heavily doped, the depletion layer becomes very narrow. Because of this, the electric field across the depletion layer becomes very narrow. Because of this, the electric field across the depletion region is very intense. The field strength is strong enough to dislodge elections from their

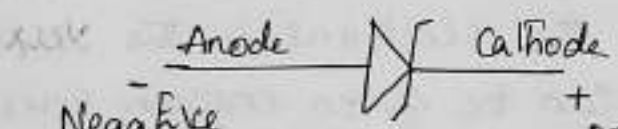
valence orbits. The creation of free electrons in this manner is known as zener effect.

Even though zener and avalanche are two different breakdown mechanisms. The term zener diode is used applied to all breakdown diodes.

Circuit Symbol:

The circuit symbol for zener diode is same as that of the ordinary diode but cathode bar is approximately in the shape of letter Z.

The arrowhead on the symbol indicates the flow of direction of forward current. Voltage drop V_Z is positive on the cathode and negative on the anode.



Negative terminal for zener operation

positive terminal for zener operation.

fig: circuit Symbol.

Zener Diode as a Voltage Regulator

Voltage regulators are the devices used to maintain constant voltage across load despite of fluctuations in the input voltage and load currents.

The zener diode in its reverse bias region is widely used as a voltage regulator as it continues to operate till the magnitude of current becomes less than $I_{Z(min)}$

The typical Zener voltage regulator as shown in fig:

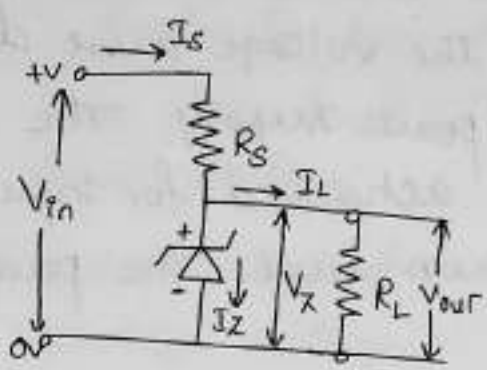


fig: Zener diode as a Voltage Regulator

The zener diode of breakdown voltage V_z is connected to the input supply in reverse direction. For all the values of current within the breakdown region, the vlg across the diode will remain fixed at V_z. giving Constant supply across the load. The resistance R_s controls the current flowing in the circuit.

Case i): When there is no load connected [I_L=0].

The current flowing in the circuit entirely passes through Zener diode. The Diode dissipates maximum power thus utmost care must be taken while selecting the series resistor so as to maintain the power dissipation within the range of maximum power dissipating capability of the diode.

Case ii) When the load resistance R_L is connected across the diode

Since the diode is parallel to the Load the vlg across the load is equal to the V_z. The Zener current must always be above $I_{Z(min)}$. The Voltage regulation can be done through two techniques i) Line Regulation.

ii) Load Regulation.

1. Line Regulation:

In this case, series resistance and load resistance are kept constant and it is assumed that all the variation in the voltage arise due to fluctuations in input power supply. The regulated output voltage is acheieved for input voltage above certain minimum level. The percentage of regulation is given by.

$$\frac{\Delta V_o}{\Delta V_{in}} \times 100.$$

where, V_o is the output vlg.

V_{in} is the input vlg.

ΔV_o is the change in the output voltage for a particular change in input voltage ΔV_{in}.

2. Load Regulation:

In this, the input voltage is fixed while the load resistance is varried. The output voltage is obtained as long as the load resistance is maintained above a minimum value. The percentage of regulation is given by.

$$= \frac{V_{No\,load} - V_{Full\,load}}{V_{Full\,load}}$$

$$= \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100$$

where,

V_{NL} = voltage across the diode when no load is applied

V_{FL} = Full load resistor voltage.

Difference between Avalanche Breakdown & Zener Breakdown.

Avalanche Breakdown	Zener Breakdown
1) Take place in lightly doped diodes	1) Take place in heavily doped diodes.
2) occurs at higher reverse voltage	2) occurs at lower reverse voltages.
3) Carrier multiplication is present	3) carrier multiplication is not present.
4) It destroys the junction	4) It will not destroy the junction
5) Depletion region is wider	5) Depletion region is small
6) It is gradual	6) It is sharp and sudden.

FORMULAE

1) o/p vlg V_o = zener vlg, V_z
   i.e $V_o = V_z$

2) current in the circuit is
   $I = I_L + I_z$

3) zener current, $I_z = I - I_L$

4) $V_i = IR + V_o$

5) $I = \frac{V_i - V_o}{R}$

6) $R = \frac{V_i - V_o}{I_z + I_L}$

7) i) $R_{min} = \frac{V_{i(max)} - V_o}{I_{z(max)} + I_{L(min)}}$

   ii) $R_{max} = \frac{V_{i(min)} - V_o}{I_{z(min)} + I_{L(max)}}$

8) $R_L = \frac{V_o}{I_L}$

9) $P_{z(max)} = I_{z(max)} V_z$

10) $I_{z(max)} = \frac{P_{z(max)}}{V_z}$

11) For $V_i(min)$: $I_Z = I_Z(min)$

$$I = I_Z(min) + I_L$$

$$\therefore V_i(min) = IR + V_o$$

12) For $V_i(max)$: $I_Z = I_Z(max)$

$$I = I_Z(max) + I_L$$

$$V_i(max) = IR + V_o$$

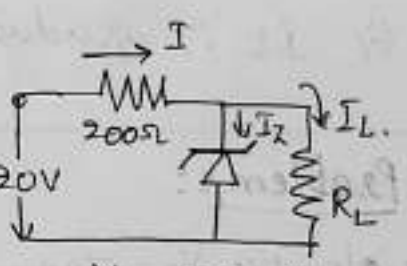
Problems:

1) For the circuit as shown in fig. zener diode is connected across the load

a) For $R_L = 180\Omega$, determine all currents & voltages

b) Repeat part (a) for $R_L = 450\Omega$

c) Find the minimum value of R_L for the zener to be in on state.



$V_Z = 10V$, $R_Z = 0$.

$P_Z(max) = 350mW$.

Soln:

a) $I = I_Z + I_L$, $V_o = V_Z$

$I_Z = 0 \Rightarrow I_L = I$

then, $I_L = \frac{20}{200+180}$

$$\boxed{I_L = 52.6mA}$$

$V_Z = V_L = 20 - (200 \times 52.6 \times 10^{-3}) = 9.48 < 10V$.

b) $R_L = 450$.

$V_L = V_Z = 10V$.

$I = \frac{20-10}{200} = 50mA$.

$I_L = \frac{V_o}{R_L} = \frac{10}{450} = 22.2mA$

$I_Z = 50 - 22.2 = 27.8mA$.

$P_Z = 27.8 \times 10 = 278mW$.

c) When the zener draws maximum power.

$$I_Z = \frac{350}{10} = 35mA.$$

Then, $I = \frac{20-10}{200} = 50mA.$

$$I_L = I - I_Z = 50 - 3.5 = 15mA.$$

$$R_L = \frac{10}{15 \times 10^{-3}} = 667\Omega.$$

d) $I_Z = 0$ (just to on state)

$I = 50mA = I_L$

$V_L = V_Z = 10V$

$$R_L = \frac{10}{50 \times 10^{-3}} = 200\Omega.$$

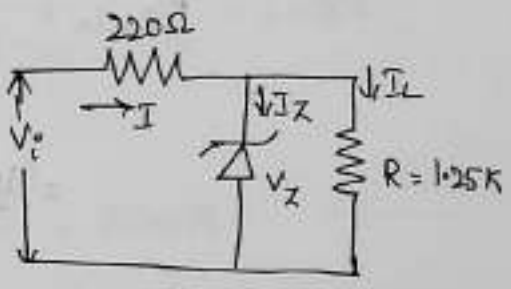
2) Determine the range of V_i which zener diode conducts.

Given: $R = 220\Omega$

$R_L = 1.25K$

$V_Z = 20V$

$P_Z = 1200mW.$



$V_Z = 20V$

$P_{Z(max)} = 1200mW.$

1) $V_Z = 20V$, $I_Z = 0$.

$$I = I_L = \frac{20}{1.25 \times 10^3} = 16mA.$$

$$V_i = 20 + 220 \times 16 \times 10^{-3} = 23.52V.$$

2) $$I_Z = I_Z(max) = \frac{1200}{20} = 60mA.$$

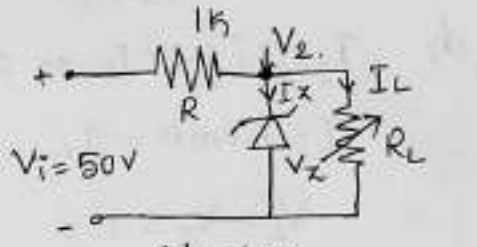
$I_L = 16mA.$

$I = 60 + 16mA = 76mA.$

$V_i = 20 + 76 \times 10^{-3} \times 280 = 36.72V.$

For input voltage from 23.52V to 36.72V. V_L will remain constant at 20V.

3) For the network shown in fig. determine the range of $R_L < I_L$ that will result in V_{R_L} being maintained at 10V. Also determine wattage rating of diode.



$V_2 = 10V$

$I_{Z(min)} = 32mA.$

Given: $R = 1K$

$V_{in} = 50V.$

$I_{Z(min)} = 32mA.$

$V_2 = 10V.$

Value of R_L, that will turn zener diode on.

$$R_{L min} = \frac{R \cdot V_2}{V_i - V_2} \quad \{\text{voltage divider}\}$$

$$= \frac{1000 \times 10}{50 - 10} = 250\Omega.$$

Voltage across R, i.e $V_R = V_i - V_2 = 50 - 10 = 40V.$

$$I = \frac{V_R}{R} = \frac{40}{1000} = 40mA.$$

$$I_{Z(min)} = I - I_{Z(max)} = 8mA.$$

$$R_{L max} = \frac{V_2}{I_{Z(min)}} = \frac{10}{8m} = 1.2K\Omega.$$

$$P_{max} = V_i I_Z = 320mW$$

4) Design a Zener regulator to meet the following specifications.

1) O/p v/g 10V 2) load current 10mA

3) Zener power, $P_{Z(max)} = 500mW$. , $I_{Z(min)} = 5mA$.

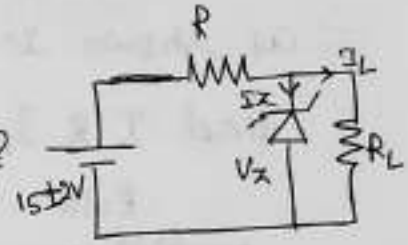
4) unregulated DC input voltage = 15 ± 2V.

Soln: Given: $V_o = V_Z = 10V$, $P_{Z(max)} = 500mW$

$I_L = 10mA$ $I_{Z(min)} = 5mA$.

$V_{i(min)} = 15 - 2 = 13V$ $R = ?$

$V_{i(max)} = 15 + 2 = 17V$. $R_L = ?$



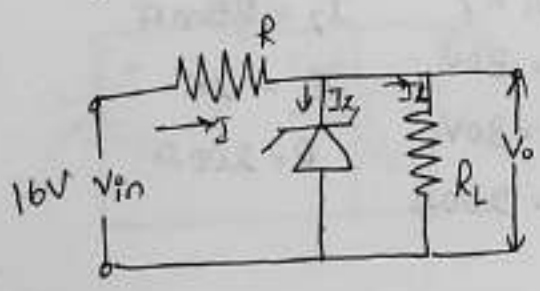
1) $R_L = \frac{V_o}{I_L} = \frac{10V}{10mA} = 1K\Omega.$

2) $R_{max} = \frac{V_{i(min)} - V_o}{I_{Z(min)} + I_{L(max)}} = \frac{13-10}{5+10} = \frac{3}{15} = 200\Omega$

3) $I_{Z(max)} = \frac{P_{Z(max)}}{V_o} = \frac{500 \times 10^{-3}}{10} = 50mA.$

$R_{min} = \frac{V_{i(max)} - V_o}{I_{Z(max)} + I_{L(min)}} = \frac{17-10}{(50+10) \times 10^{-3}} = 116\Omega.$

5) Find the value of Resistance 'R' in the circuit shown in fig. when the voltage across the Zener is 10V and the Zener current is 20mA.



Given: $V_Z = 10V$, $I_Z = 20mA$, $R_L = 1K$.

$V_o = V_Z = 10V$.

1) $I_L R_L = 10V$

$I_L = \frac{10V}{1 \times 10^3} = 10mA.$

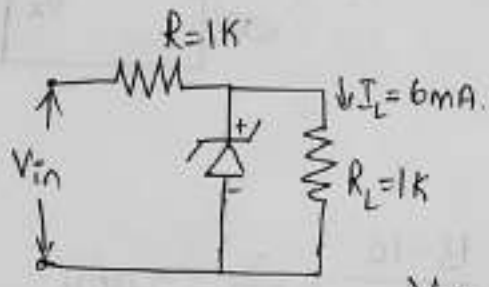
$I = I_L + I_Z$

$= 10 + 20 = 30mA.$

$I = \frac{V_i - V_o}{R} \Rightarrow R = \frac{V_i - V_o}{I} = \frac{16-10}{30 \times 10^{-3}}$

$\boxed{R = 200\Omega}$

6) A 10V zener is connected for voltage regulator as shown in fig. If the load current is 6mA. find I & I_Z.



$V_o = I_L R_L$

$V_o = 6 \times 10^{-3} \times 1 \times 10^{3} = 6V.$

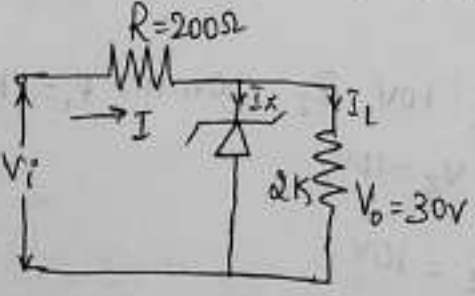
$\boxed{V_L = V_o = 6V}$

$V_Z = 6V \therefore I_Z = 0$ & $I = 6mA$

$I = I_L + I_Z = 6mA.$

→ Since diode is in parallel with R_L, the device is 10V zener. it cannot conduct and is open.

7. Over what range of input v/g will the zener circuit shown in figure maintain 30V across 200Ω load assuming that series resistance R = 200Ω and the zener current rating is 25mA.



Given: V_i = ?

$V_o = 30V$

$V_Z = 30V$

$R = 200\Omega$

$I_Z = 25mA.$

$R_L = 2K$

$R = 200\Omega.$

1) The minimum i/p vlg is required will be when $I_Z = 0$ and $I = I_L$.

$$I_L = \frac{V_o}{R_L} = \frac{30}{2K} = 15mA.$$

$\therefore$ $\boxed{I_L = 15mA.}$

$\therefore$ Minimum i/p vlg $= V_o + IR$

$= 30 + (15 \times 10^{-3} \times 200)$

$= 30 + 3$

$\boxed{V_{i(min)} = 33V.}$

2) when $I_Z = max$. i.e $I_Z = 25mA$.

$I = I_L + I_Z = 15 + 25m = 40mA.$

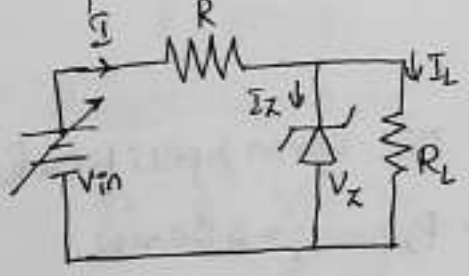
maximum i/p vlg $= V_o + IR$

$= 30 + (40 \times 10^{-3}) \times 200$

$\boxed{V_{i(max)} = 38V}$

$\therefore$ input voltage range is $\boxed{33V \text{ to } 38V}$ to get 30V.

3) A zener diode shown in fig has $V_Z = 18V$ The vlg across the load stays at 18V as long as I_Z is maintained b/w 200mA and 2A. Find the value of Series resistance so that V_o remains 18V while the input voltage V_i is free to vary from 22V to 28V.



Given: $V_Z = 18V$ $R = ?$

$I_{Z(min)} = 200mA$ $V_o = 18V$

$I_{Z(max)} = 2A.$

$V_{i(min)} = 22V$ $V_{i(max)} = 28V$

$I_{z(min)} = 200mA$ when $V_i(min) = 22V$.

$\therefore I_L$ remain unchanged.

$$\therefore I_L = \frac{V_o}{R_L} = \frac{18V}{18\Omega} = 1A = 1000mA.$$

$$R = \frac{V_{in} - V_o}{I_z + I_L} = \frac{22 - 18}{(200 + 1000) \times 10^{-3}}$$

$$\boxed{R = 3.33\Omega}$$

9) Design a Zener Regulator for the given specification

i) i/p DC is $10V \pm 2V$

ii) o/p requirements are 5V, 20mA.

iii) Assume $I_{z(min)} = 5mA$, $I_{z(max)} = 80mA$.

Given: $V_z = V_o = 5V$

$I_L = 20mA$

$I_z = 5mA$ when $V_{in} = 10 - 2V = 8V$

$I_z = 80mA$ when $V_{in} = 10 + 2 = 12V$.

* $I_L = 20mA$ and voltage across the load $V_o = 5V$. The load current stays constant

i.e $I_L = \frac{V_o}{R_L} \Rightarrow R_L = \frac{5}{20mA} = 250\Omega$

Series Resistance

$$R = \frac{V_{in} - V_o}{I_{z(min)} + I_L} = \frac{8 - 5}{(5 + 20) \times 10^{-3}} = \frac{3}{25 \times 10^{-3}}$$

$$\boxed{R = 120\Omega}$$

10) Design a zener Regulator for the given specification

i) o/p v/g = 5V ii) $I_L = 10mA$ iii) $P_{z(max)} = 400mW$

iv) i/p v/g = $10V \pm 2V$

Soln: Given: $V_0 = V_Z = 5V$

$I_L = 10mA$

$P_{Z(max)} = 400mW$

$V_i(min) = 10-2 = 8V$

$V_i(max) = 10+2 = 12V.$

$$R_L = \frac{V_0}{I_L} = \frac{5}{10 \times 10^{-3}} = 0.5k$$

$R_L = 500\Omega$

max zener current. $I_{Z(max)} = \frac{400mW}{5V} = 80mA$

Minimum i/p v/g required when $I_Z = 0$

$I = I_L = 10mA.$

$V_i(min) = 10-2 = 8V$

$V_i(max) = 10+2 = 12V$

$$R_{min} = \frac{V_{i(max)} - V_0}{I_{Z(max)} + I_L}$$

$$= \frac{12-5}{90mA} = 77.7\Omega$$

$$R_{max} = \frac{V_{L(min)} - V_0}{10+0} = \frac{8-5}{10mA} = 300\Omega.$$

$\therefore$ $77.7 < R < 300\Omega$ to get $V_0 = 5V.$

(11) A 24V, 600mW zener diode is used for providing a 24V stabilized supply to a variable load. If the input voltage is 32V. Calculate

i) The value of series resistance required

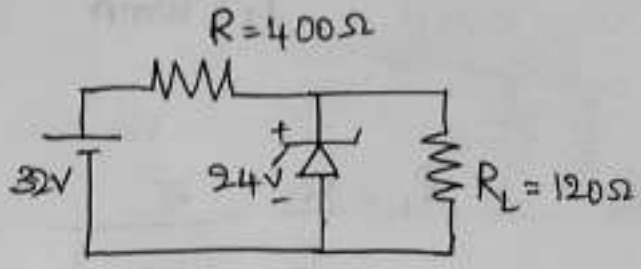
ii) Diode current when the load is 1200Ω and $R = 400\Omega.$

Given: $V_Z = 24V$, $P_{Z(max)} = 600mW$, $V_0 = 24V$, $V_i = 32V.$

i) $$R = \frac{V_{in} - V_Z}{I_Z + I_L}$$

I_L & R_L is not given, so $I_L = 0$

$$\therefore R = \frac{V_{in} - V_2}{I_{Z(max)}}$$



$$P_{Z(max)} = I_{Z(max)} \cdot V_Z$$

$$I_{Z(max)} = \frac{P_{Z(max)}}{V_Z} = \frac{600mW}{24} = 25mA$$

$$R = \frac{32V - 24V}{25mA} = 32\Omega$$

2) When load is 1200Ω & R = 400Ω

$$I_L = \frac{V_o}{R_L} = \frac{24V}{1200\Omega} = 20mA.$$

$$I = \frac{V_{in} - V_o}{R} = \frac{32V - 20}{400\Omega} = 20mA$$

$$I = I_Z + I_L$$

$$I_Z = I - I_L = 20 - 20 = 0 \Rightarrow \boxed{I_Z = 0}$$

when $R_L = 1200\Omega$, current $I_Z = 0A$.

12) Design the zener regulator for the following specification

1) O/p vlg = 5V 2) I_L = 20mA 3) $P_{Z max}$ = 500mW

4) I/p voltage = 125 ± 3V.

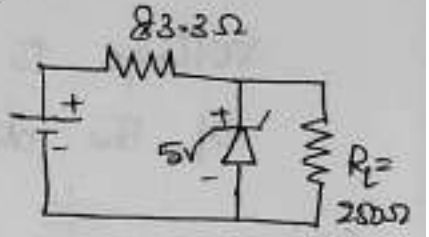
Given: $V_o = 5V$, $V_Z = 5V$, $I_L = 20mA$, $P_{Z(max)} = 500mW$

$V_{i(min)} = 122V$ $V_{i(max)} = 128V$.

1) $R_L = \frac{V_o}{I_L} = \frac{5V}{20mA} = 250\Omega$

2) $I_{z(max)} = \frac{P_{z(max)}}{V_z} = \frac{500mW}{5V} = 100mA$

3) $R_{min} = \frac{V_{i(max)} - V_o}{I_{z(max)} + I_{L(min)}} = \frac{15V - 5V}{100m + 20m}$



$R_{min} = 83.33\Omega$

13) In a zener diode regulator, the input DC is 10V ± 2V. The output requirement are 5V and 20mA. Assuming $I_{z(min)}$ & $I_{z(max)}$ as 5mA and 80mA. Design the zener diode regulator.

Given: $V_{in} = 10V \pm 2V$

$V_o = V_z = 5V$

$I_L = 20mA$

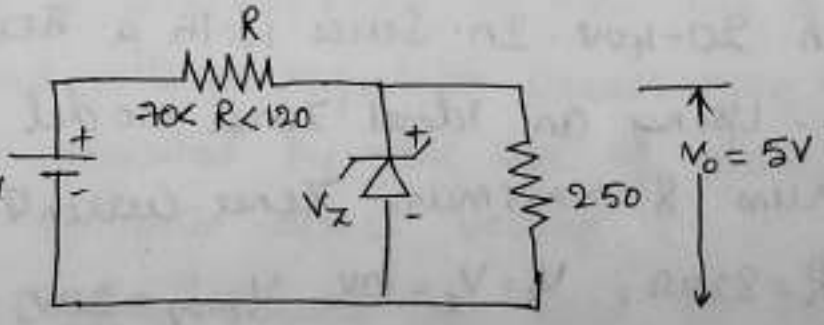
$I_{z(max)} = 80mA$

$I_{z(min)} = 5mA$

1) $R_L = \frac{V_o}{I_L} = \frac{5V}{20mA} = 250\Omega$

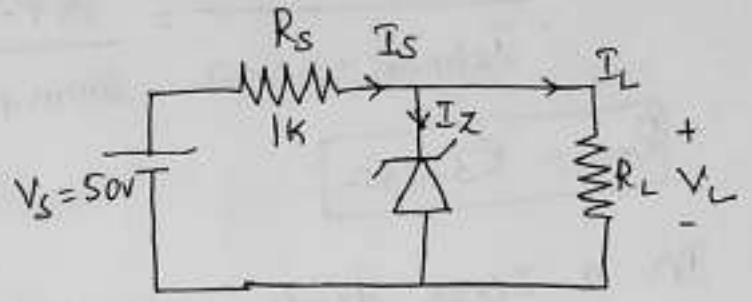
2) $R_{min} = \frac{V_{i(max)} - V_o}{I_{z(max)} + I_{L(min)}} = \frac{12V - 5V}{80m + 20m} = 70\Omega$

3) $R_{max} = \frac{V_{i(min)} - V_o}{I_{z(min)} + I_{L(max)}} = \frac{8V - 5V}{(5 + 20) \times 10^{-3}} = 120\Omega$



14) In the zener voltage regulator shown in fig. Zener rating are $V_z = 10V$ at a current of 32mA

$R_z = 0$. Find the range of R_L and I_L for load voltage to be constant. what is the maximum vlg of the diode.



Given:

$V_0 = V_z = 10V$.

$I_z = 32mA$

$R_z = 0$, $V_{in} = 50V$, $R = 1K$ $R_L = ?$, $P_{z(max)} = ?$

$$I = \frac{V_{in} - V_0}{R} = \frac{50V - 10V}{1K} = 40mA.$$

$$I = I_z + I_L \Rightarrow I_L = I - I_z = 40m - 32m$$

$$I_L = 8mA$$

$$R_L = \frac{V_0}{I_L} = \frac{10V}{8mA} = 1250\Omega$$

$$P_{z(max)} = I_z V_0 = 32m \times 10V$$

$$\boxed{P_{z(max)} = 320mW}$$

15) A zener diode has a breakdown voltage of 10V. It is supplied from a voltage source varying between 20-40V. In series with a resistance of 820Ω. Using an ideal zener model obtain the minimum & maximum zener current.

Given: $R = 820\Omega$, $V_0 = V_z = 10V$, $V_{i(min)} = 20V$, $V_{i(max)} = 40V$.

$$I_{min} = \frac{V_{i(min)} - V_0}{R} = \frac{20V - 10V}{820\Omega} = 12.195mA.$$

$$I_{max} = \frac{V_{i(max)} - V_o}{R} = \frac{40V - 10V}{820\Omega} = 36.585\,mA.$$

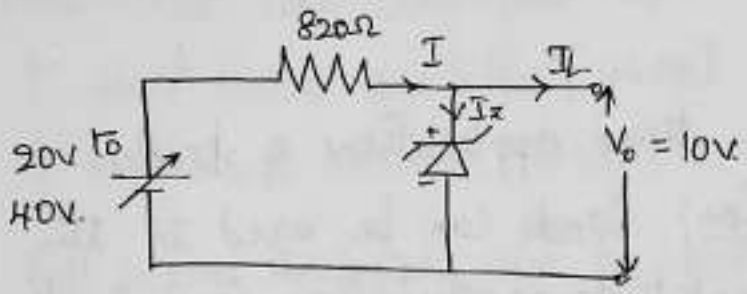
for ideal zener model, $I_{Z(min)} = 0A$.

$I_{L(min)} = 0A$, when o/p terminals are open

$$I_{max} = I_{Z(max)} + I_{L(min)}$$

$$I_{max} = I_{Z(max)}$$

$$\therefore I_{Z(max)} = I_{max} = 36.585\,mA.$$



Applications of Diodes

One of the most important applications of diodes is rectification. other applications include clipping, clamping, dc voltage multiplication, and logic circuits.

* Rectification is the process of converting an ac voltage to dc voltage i.e conversion of sinusoidal ac waveforms into single polarity half cycles. This can be accomplished by the use of rectifiers, filters and voltage regulator circuit. The rectified wave is smoothed by the use of capacitors to procen it into direct voltage.
* Diode clipping circuits are used for clipping-off an unwanted portion of a waveform.

* clamping circuits change the dc level of a waveform without affecting the wave shape. i.e clamping circuits shifts the signal either to the +ve side & negative side of the axis.
* DC voltage multipliers are applied to change the level of a dc voltage source to a desired high level
* Logic circuits produce a high & low o/p vlgs. depending upon the voltage levels at several i/p terminals.

These are few real time applications of Diodes.

1) Radio Demodulation: Diode can be used in the demodulation of amplitude modulation (AM) radio broadcasts. The Diode rectifies the AM signal, leaving a signal whose average amplitude is the desired audio signal. The average value is extracted using a simples filter. and fed into an audio transducer. which generates sound.

2) Over-voltage protection: Diodes are also used as protection devices for sensitive electronic components. Specialized diodes called transient voltage suppressors are designed specifically for over voltage protection and can handle very large power spikes for short time periods.

3) Limiter: This circuit limits output swing to one diode drop roughly 0.7V. This diode limiters is often used as i/p protection for high gain amplifier.

Rectifiers:

Rectification: Rectification is the process of converting alternating current (ac) to direct current (dc).

Rectifier:

Rectifier is a device that converts ac (alternating current) into dc (direct current). Semiconductor diodes are used as rectifying elements.

Rectifiers are classified as:

1. Half wave rectifier [HWR]
2. Full wave rectifier [FWR]

Full wave rectifier can be built in two ways:

1. Full-wave rectifier using two diodes and a centre tapped transformer → Centre tapped full wave rectifier [CTFW]
2. Full-Wave Bridge rectifier using four diodes and an ordinary transformer → Full Wave Bridge Rectifier [FWBR].

Half Wave Rectifier [HWR]

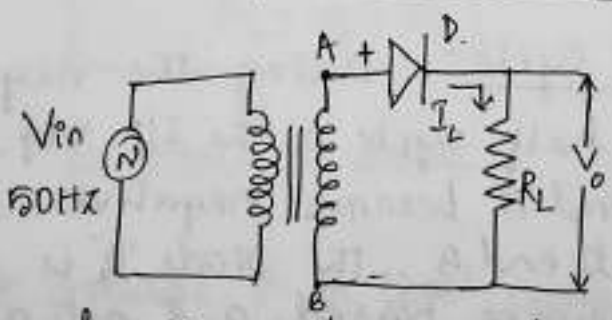
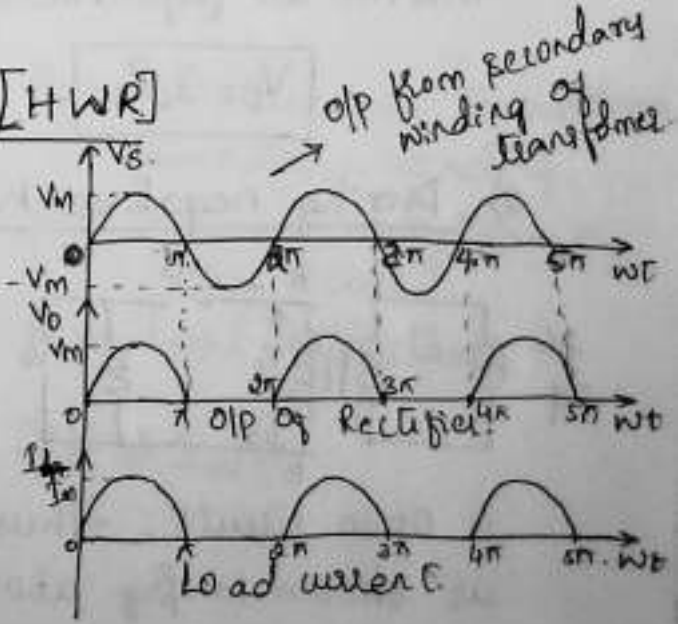


fig: Circuit diagram for Half wave Rectifier



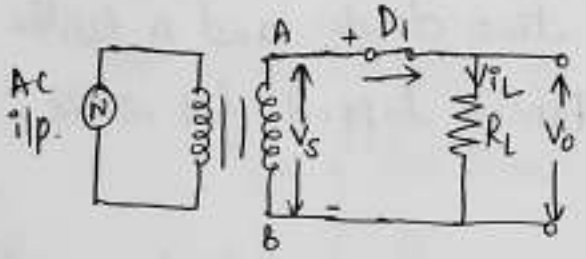
In almost all the rectifiers circuits, transformers are generally used for following purposes.

1) Either to step up & step down the input vlg.
2) To provide better isolation between AC supply and rectifier circuit.

Half wave rectifier circuit is as shown in figure above. It consists of a single diode in series with load resistance. The ac voltage across the secondary winding A & B changes polarities after half cycle.

Operation:

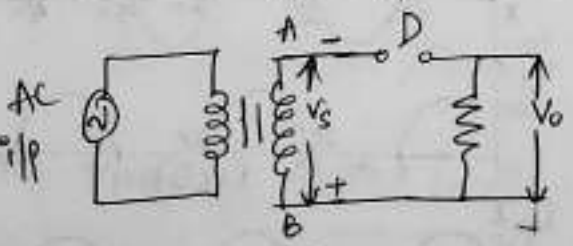
1) During +ve half cycle:



During the positive half cycle of the ac input vlg. end A becomes positive with respect to end B. The diode 'D_1' is forward biased and acts as a short circuit, thus the current flows in the circuit as shown in fig. The load voltage is given by

$$V_o = I_L R_L \quad \& \quad V_o = V_{in}$$

2) During negative half cycle: During the negative half cycle of the i/p vlg. end A becomes negative w.r.t to end B, the Diode 'D_1' is reverse biased and acts as a open circuit, thus no current flows in the circuit as shown in fig above. The load vlg is given by $V_o = 0$



Let the I/p equation of the alternating secondary voltage is.

$$\boxed{V_s = V_m \sin \omega t}$$

∴ The o/p of the rectifier is defined as

$$V_o = \begin{cases} V_m \sin \omega t & : 0 \le \omega t \le \pi \\ 0 & ; \pi \le \omega t \le 2\pi. \end{cases}$$

The output waveform is expected to be a straight line but half wave rectifier gives output in the form of positive sinusoidal pulses. Hence the output is called pulsating dc.

The load current is given by.

$$I_L = \begin{cases} I_m \sin \omega t & : 0 \le \omega t < \pi \\ 0 & ; \pi \le \omega t \le 2\pi \end{cases}$$

where $\boxed{I_m = \frac{V_m}{R_L}}$ → ideal diode. V_m → peak value of the o/p.

$\boxed{I_m = \frac{V_m}{R_L + r_d + R_s}}$ ↓ for practical diode.

where, R_s → Resistance of transformer secondary winding

r_d → Dynamic resistance of the diode

R_L → Load resistance

1) Average & DC Load current (I_{dc} & I_{av}).

$$I_{dc} = \frac{1}{2\pi} \int_0^{2\pi} I_L \cdot d(\omega t)$$

$$= \frac{1}{2\pi}\left[\int_0^{\pi} I_m \sin\omega t \, d\omega t + \int_{\pi}^{2\pi} 0 \cdot d\omega t\right]$$

$$= \frac{1}{2\pi}\left[\int_0^{\pi} I_m \sin\omega t \cdot d\omega t\right]$$

$$= \frac{I_m}{2\pi}\left[-\cos\omega t\right]_0^{\pi} = -\frac{I_m}{2\pi}[-1-1]$$

$$= -\frac{I_m}{2\pi}[-2]$$

$$\boxed{I_{dc} = \frac{I_m}{\pi}}$$

2) Average dc load voltage [V_{dc}]

$$V_{dc} = I_{dc} \cdot R_L$$

$$= \frac{I_m}{\pi} \cdot R_L$$

$$= \frac{V_m}{R_L \cdot \pi} \cdot R_L \qquad \left[\because I_m = \frac{V_m}{R_L}\right]$$

$$\boxed{V_{dc} = \frac{V_m}{\pi}}$$

3) RMS value of Load current (I_{RMS}):

$$I_{RMS} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} I_L^2 \cdot d\omega t}$$

$$= \sqrt{\frac{1}{2\pi}\int_0^{\pi} (I_L)^2 d\omega t + \int_{\pi}^{2\pi} I_L^2 d\omega t}$$

$$= \left[\frac{1}{2\pi}\int_0^{\pi} I_m^2 \sin^2\omega t \, d\omega t + \int_{\pi}^{2\pi} 0 \cdot d\omega t\right]^{1/2}$$

$$= \left[\frac{I_m^2}{2\pi}\int_0^{\pi} \sin^2 \omega t \, d(\omega t)\right]^{1/2}$$

$$= \left[\frac{I_m^2}{2\pi}\int_0^{\pi} \frac{1-\cos 2\omega t}{2} \, d\omega t\right]^{1/2}$$

$$= \left[\frac{I_m^2}{2\pi}\left[\frac{\omega t}{2} - \frac{\sin 2\omega t}{4}\right]_0^{\pi}\right]^{1/2}$$

$$= \left[\frac{I_m^2}{2\pi}\left[\left[\frac{\pi}{2} - 0\right] - \left[\frac{\sin 2\pi}{4} - \frac{\sin 2(0)}{4}\right]\right]\right]^{1/2}$$

$$= \sqrt{\frac{I_m^2}{2\pi}\left[\frac{\pi}{2}\right]} = \sqrt{\frac{I_m^2}{4}}$$

$$\boxed{I_{RMS} = \frac{I_m}{2}}$$

4) RMS value of the load voltage $[V_{RMS}]$

$$V_{RMS} = I_{RMS} \cdot R_L$$

$$= \frac{I_m}{2} \cdot R_L \qquad I_m = \frac{V_m}{R_L}$$

$$= \frac{V_m}{R_L \cdot 2} \cdot R_L$$

$$\boxed{V_{RMS} = \frac{V_m}{2}}$$

5) DC output power $[P_{dc}]$

$$P_{dc} = I_{dc}^2 \cdot R_L$$

$$= \left(\frac{I_m}{\pi}\right)^2 \cdot R_L = \frac{I_m^2}{\pi^2} \cdot R_L$$

$$= \left(\frac{V_m}{R_L}\right)^2 \cdot \frac{1}{\pi^2} \cdot R_L$$

$$= \frac{V_m^2}{R_L^2 \cdot \pi^2} \cdot R_L$$

$$\boxed{P_{dc} = \left(\frac{V_m}{\pi}\right)^2 \cdot \frac{1}{R_L}}$$

6) Ac output power (P_{ac})

$$P_{ac} = I_{rms}^2 \cdot R_L$$

$$\boxed{P_{ac} = \left(\frac{I_m}{2}\right)^2 \cdot R_L}$$

⇒ Rectifier Efficiency

The efficiency of rectifier is defined as the ratio of the o/p power to the total amount of i/p power supplied to the circuit.

Efficiency, $\eta = \frac{\text{d.c delivered power to load}}{\text{a.c i/p power from transformer secondary.}}$

$$\eta = \frac{P_{dc}}{P_{ac}}$$

$$= \frac{\frac{I_m^2}{\pi^2} \cdot R_L}{\frac{I_m^2}{4} \cdot R_L} = \frac{\frac{1}{\pi^2}}{\frac{1}{4}}$$

$$\eta = \frac{4}{\pi^2}$$

$$\therefore \eta = 0.406$$

$$\boxed{\% \eta = 40.6\%}$$

$\eta = 40.6\%$ indicates that, under the most ideal conditions, only 40.6% of the a.c i/p power is converted into dc power in the load. The remaining exists as a.c power.

8) Ripple Factor

The residual pulsation in the direct current from a rectifier is called a ripple. A measure of the smoothness of the d.c o/p of a rectifier is called a ripple factor, γ. Ripple factor indicates how successfully a circuit is in converting the a.c to d.c. This is defined as,

$$\text{Ripple factor} = \gamma = \frac{\text{effective (r.m.s) value of a.c component}}{\text{average or d.c components.}}$$

The requirement of a rectifier is to minimize its ripple factor (ripple content). This is achieved by introducing a filter in the rectifier o/p. Thus, a filter converts a pulsating o/p from a rectifier into a very steady state d.c output & it filters out & smoothens out the pulsations at the output.

If I_{ac} is the effecting value of the a.c components, then the total load current is the RMS value of the i_L is,

$$I_{RMS} = \sqrt{I_{dc}^2 + I_{ac}^2} \Rightarrow I_{RMS}^2 = I_{dc}^2 + I_{ac}^2$$

$$I_{ac} = \sqrt{I_{RMS}^2 - I_{dc}^2}$$

Ripple factor, $\boxed{\gamma = \frac{I_{ac}}{I_{dc}}} = \frac{\sqrt{I_{RMS}^2 - I_{dc}^2}}{I_{dc}}$

$$\gamma = \sqrt{\frac{I_{RMS}^2 - I_{dc}^2}{I_{dc}^2}}$$

$$= \sqrt{\frac{I_{RMS}^2}{I_{dc}^2} - 1}$$

$$= \sqrt{\left(\frac{I_m/2}{I_m/\pi}\right)^2 - 1} = \sqrt{\frac{\pi^2}{4} - 1}$$

$\boxed{\gamma = 1.21}$ → This indicates in % the amount of a.c present in the o/p is 121% of the d.c voltage

Peak Inverse Voltage [PIV]

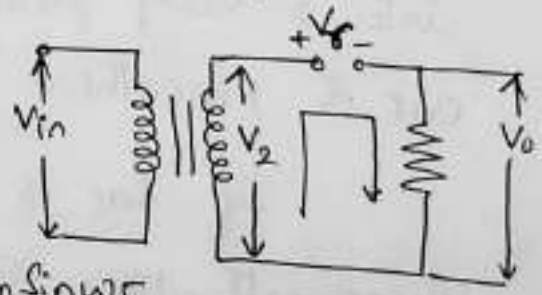
PIV is the maximum voltage across the diode, when the diode is reverse biased.

Applying KVL to the ckt,

$$-V_2 + V_\gamma - I_L R_L = 0$$

$$-V_2 + V_\gamma - 0 \times R_L = 0$$

$\boxed{V_\gamma = V_2}$



$V_2 = V_m \sin\omega t$

$\boxed{V_\gamma max = V_m}$ $(\sin\omega t)_{max} = 1$

Therefore for HWR, $\boxed{PIV = V_m}$

10) **Voltage Regulation**

Regulation is defined as the variation in DC output voltage as a function of DC current.

$$\% \text{ Regulation} = \frac{V_{NO\,LOAD} - V_{FULL\,LOAD}}{V_{FULL\,LOAD}}$$

If % regulation is zero then PT is ideal rectifier but in actual practice

$$\% \text{ Regulation} = \frac{R_s + R_f}{R_L} \times 100$$

$$\% \text{ Regulation} = \frac{R_f}{R_L} \times 100$$

Advantages:

1. The circuit is simpler and requires only one diode.
2. PIV is only V_m.
3. Centre tap transformer is not neccessary.

Disadvantages:

1. Ripple factor $\gamma = 121\%$ is too high.
2. Efficiency is very low about 40.6% but practice value is still less.
3. Low transformer utilization factor = 0.287.
4. Because of all these disadvantages HWR is not used as power rectifier.

Note: Transformer utilization factor [TUF]: It is defined as the ratio of dc power delivered to the load to the ac power rating of the transformer.

Full-Wave Rectifier

The disadvantages of a half wave rectifier are reduced & eliminated by the use of another diode. Here both the half cycles of the input are utilized and is used with the centre tapped transformer.

A full wave rectifier circuit with two diodes and a centre-tapped transformer is as shown in fig.

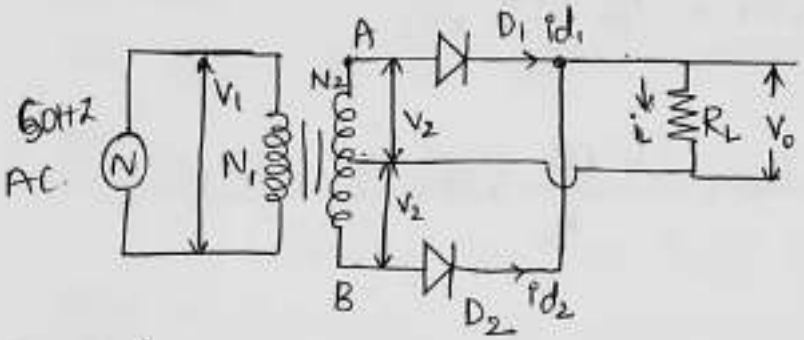


fig: Centre tapped full wave rectifier.

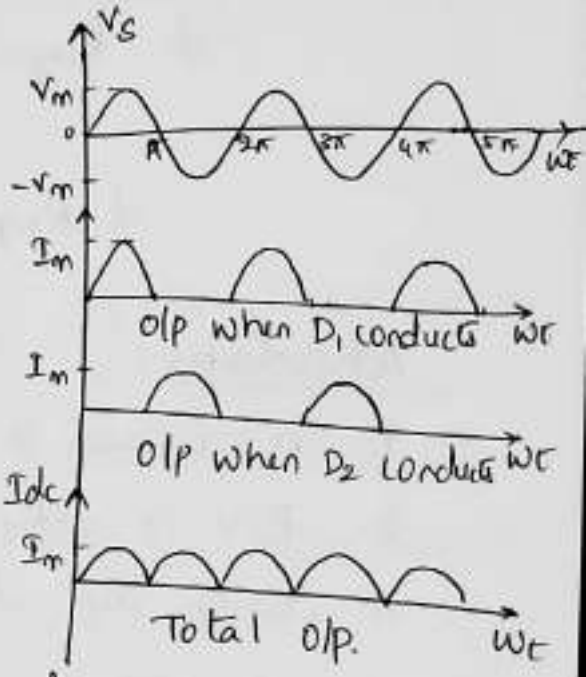


fig: i/p-o/p waveform of Full wave

When the i/p ac supply is switched on, the ends A & B of the transformer secondary becomes +ve & -ve alternatively.

Operation:

During +ve half cycle: During +ve half cycle of the ac input voltage, end A becomes +ve with respect to end B, the diode 'D_1' is forward biased and conducts while the diode D_2 is reverse biased and acts as open circuit and conducts while the other diode D_2 is reverse biased and acts as an open circuit and will not conduct as shown in fig below.

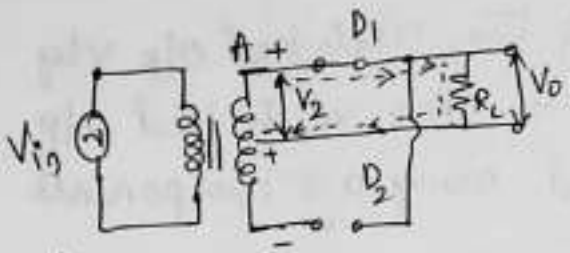


fig: During +ve half cycle.

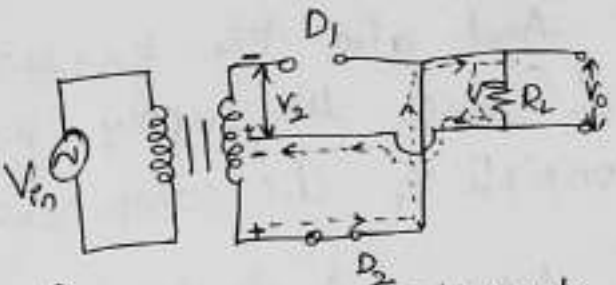


fig: During -ve half cycle.

The Diode D_1 supplies the load current. The conventional current flow is through D_1, load resistor R_L and the upper half of the secondary winding as shown by the dotted arrows.

During the -ve half cycle:

During the -ve half cycle of the input ac vlg, end A becomes -ve with respect to end B. the diode 'D_2' is forward biased and conducts while the diode 'D_1' is reverse biased and acts as open circuit and will not conduct as shown in fig above.

The diode D_2 supplies the load current. The conventional current flow is through diode D_2, load resistor R_L and the lower half of the secondary winding as shown by the dotted lines in the figure above.

As seen from the two figures above, the current in the load R_L is in the same direction for both half cycles of ac i/p vlg.

For both the half cycles the current flows through the load in the same direction Hence we get two half cycles for one complete input signal.

And also the frequency of the rectified o/p v/g is twice the supply frequency. The rectified o/p consists of d.c components and many a.c components.

1) **Average & dc Load Current [Idc]**

Considering one cycle of the load current I_L from 0 to π to obtain the average value which is dc value of load current.

$$I_{dc} = \frac{1}{\pi}\int_0^{\pi} I_L \cdot d\omega t$$

$$= \frac{1}{\pi}\int_0^{\pi} I_m \cdot \sin \omega t \, d\omega t.$$

$$= \frac{I_m}{\pi}\left[-\cos \omega t\right]_0^{\pi}$$

$$= \frac{I_m}{\pi}\left[-\cos \pi - (-\cos 0)\right] = \frac{I_m}{\pi}(2)$$

$$\boxed{I_{dc} = \frac{2I_m}{\pi}}$$

2) **Average dc load voltage: [Vdc]**

$$V_{dc} = I_{dc} \cdot R_L$$

$$= \frac{2I_m}{\pi} \cdot R_L = \frac{2V_m}{\pi \cdot R_L} \cdot R_L$$

$$\boxed{V_{dc} = \frac{2V_m}{\pi}}$$

$$I_{dc} = \frac{2I_m}{\pi}$$

$$I_m = \frac{V_m}{R_L}$$

3) **RMS value of Load Current (I_{rms}):**

$$I_{rms} = \sqrt{\frac{1}{\pi}\int_0^{\pi} I_L^2 \cdot d\omega t}$$

$$= \sqrt{\frac{1}{\pi}\int_0^{\pi} I_m^2 \cdot \sin^2 \omega t \cdot d\omega t}$$

$$= \sqrt{\frac{I_m^2}{\pi}\int_0^{\pi} \frac{1-\cos 2\omega t}{2} \cdot d\omega t} \qquad \because \int \sin^2\theta = \frac{1-\cos 2\theta}{2}$$

$$= \sqrt{\frac{I_m^2}{\pi}\left[\frac{\omega t}{2} - \frac{\sin 2\omega t}{4}\right]_0^{\pi}} \qquad \because \int \cos 2\theta = \frac{\sin 2\theta}{2}$$

$$= \sqrt{\frac{I_m^2}{2\pi}\{\pi - 0\} - \frac{1}{2}[\sin 2\pi - \sin(0)}$$

$$= \sqrt{\frac{I_m^2}{2}}$$

$$\boxed{I_{RMS} = \frac{I_m}{\sqrt{2}}}$$

4) RMS value of the Load Voltage (V_{RMS})

$$V_{RMS} = I_{RMS} \cdot R_L$$

$$= \frac{I_m}{\sqrt{2}} \cdot R_L$$

$$\boxed{V_{RMS} = \frac{V_m}{\sqrt{2}}}$$

5) Dc output power [P_{dc}]:

$$P_{dc} = I_{dc}^2 \cdot R_L$$

$$= \left(\frac{2I_m}{\pi}\right)^2 \cdot R_L$$

$$\boxed{P_{dc} = \frac{4I_m^2}{\pi^2} \cdot R_L}$$

6) AC output power [P_{ac}]

$$P_{ac} = I_{RMS}^2 \cdot R_L$$

$$= \left(\frac{I_m}{\sqrt{2}}\right)^2 \cdot R_L$$

$$\boxed{P_{ac} = \frac{I_m^2}{2} \cdot R_L}$$

7) Rectification Efficiency: [η]

$$\eta = \frac{P_{dc}}{P_{ac}}$$

$$= \frac{4/\pi^2 \cdot R_L \cdot I_m^2}{\frac{I_m^2}{2} \cdot R_L} = \frac{4}{\pi^2} \times \frac{2}{1}$$

$$\eta = \frac{8}{\pi^2}$$

$$\% \eta = 81.2\ \%$$

8) Ripple factor (γ):

$$\gamma = \sqrt{\frac{I_{rms}^2}{I_{dc}^2} - 1}$$

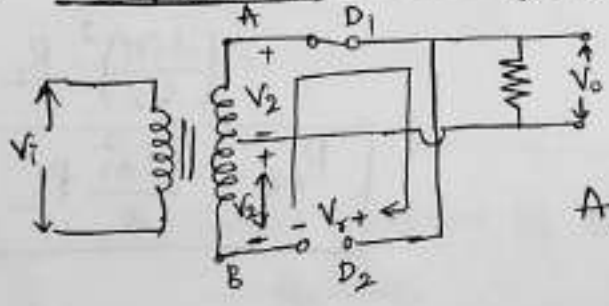
$$\gamma = \sqrt{\left[\frac{(I_m/\sqrt{2})^2}{(2I_m/\pi)^2}\right] - 1} = \sqrt{\left(\frac{1/2}{4/\pi^2}\right) - 1}$$

$$= \sqrt{\left(\frac{1}{2} \times \frac{\pi^2}{4}\right) - 1} = \sqrt{\frac{\pi^2}{8} - 1}$$

$$\gamma = 0.48$$

This indicates that the amount of ac present in the output is 0.48 % of the dc voltage.

9) Peak Inverse Voltage (PIV)



PIV is the maximum vlg across the diode, when the diode is reverse biased

Applying KVL,

$$+V_2 + V_2 - V_\gamma = 0$$

$$V_\gamma = 2V_2$$

$$PIV = 2V_m$$

Advantages of FWR.

1) The efficiency is twice that of HWR i.e 81.2%.
2) The ripple factor is much less than that of HWR
3) The dc o/p output voltage and load current value are twice than HWR.
4) Large dc output
5) Full 100% of the input is utilized

Disadvantages of FWR.

1) PIV of the diode is higher.
2) Cost of centre tap transformer is higher.
3) Output voltage is half of the secondary voltage.

FULL WAVE BRIDGE RECTIFIER

Bridge Rectifier is the most frequently used circuit for electronic d.c power supplies. Four Diodes are used. but the transformer used is not centre tapped and gives output of V_2. The circuit diagram for Bridge rectifier and the respective waveforms are as shown in fig below.

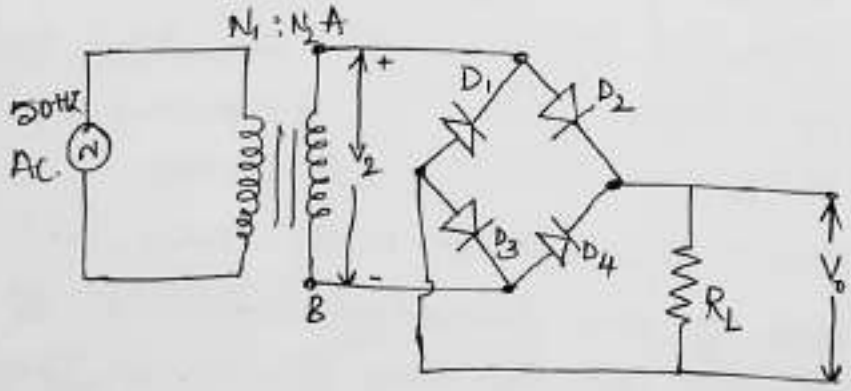
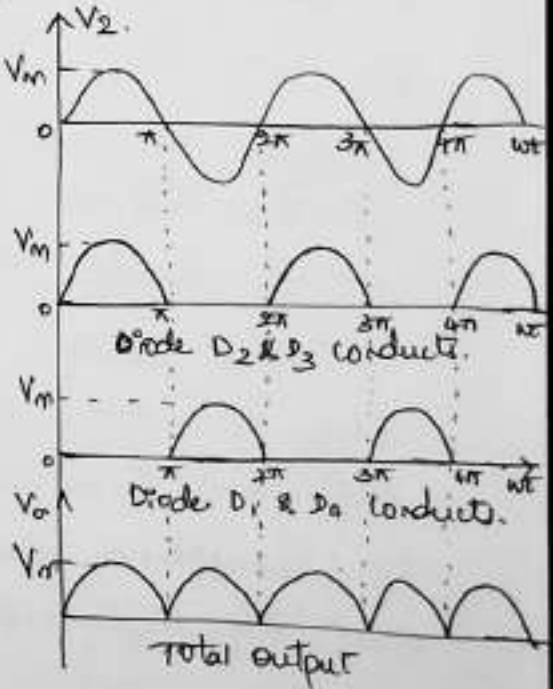
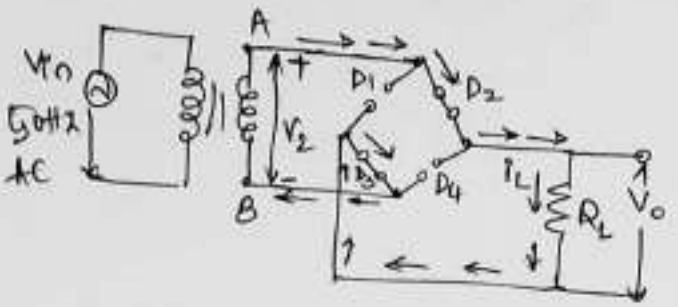


fig: Circuit diagram of Bridge Rectifier.

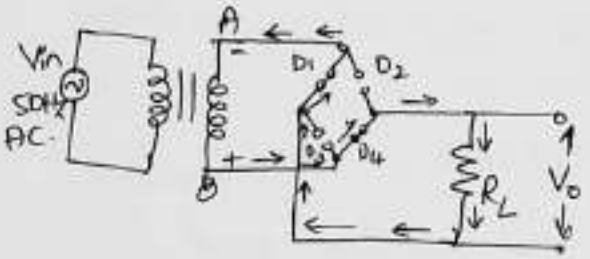


During +ve half cycle:



During +ve half cycle of the i/p end A becomes +ve with respect to end B. This makes Diode D_2 & D_3 forward biased and the diodes D_1 & D_4 reverse biased. Therefore only diodes D_2 & D_3 conducts during the +ve half cycle of the input. The conventional current flows through the load resistance R_L as shown in figure producing the drop across R_L.

During -ve half cycle.



During -ve half cycle of the i/p end A becomes -ve with respect to end B. This makes Diode D_1 & D_4 forward biased and the diodes D_2 & D_3 reverse biased. Therefore only diodes D_1 & D_4 conducts during the -ve half cycle of the input. The conventional current flows through the load resistance R_L as shown in fig. producing the drop across the R_L.

For both the half cycles the current flows through load in the same direction. Hence we get two half cycles for one complete input signal. i.e The frequency of the o/p is double that of the i/p supply frequency.

The Bridge circuit transformer needs only half the secondary turns of the transformer compared to full wave rectifier circuit for the same dc o/p voltage. i.e transformer secondary line-to-line v/g should be one half that used for the full wave rectifier.

Advantages of FWBR:

1) The need for centre tapped transformer is eliminated
2) The PIV is only V_m.
3) The transformer is less costly.

Disadvantages of FWBR:

1) It requires four diodes, causing an additional voltage drop that reduces the o/p v/g.

Applications of Rectifiers:

1) In power supply circuits.
2) In rectifier type meter to convert ac voltage to be measured to DC.

Comparision of Rectifier circuits.

parameter	HWR	FWR	FWBR.
1) Peak voltage	$V_m = \sqrt{2}\, V_2$ $= \sqrt{2} \times V_S$	$V_m = \sqrt{2}\, V_2$ $V_m = \sqrt{2} \times V_S$	$V_m = \sqrt{2} \cdot V_2$ $= \sqrt{2} \cdot V_S$.
2) Peak load current [Ideal]	$I_m = \frac{V_m}{R_L}$	$I_m = \frac{V_m}{R_L}$	$I_m = \frac{V_m}{R_L}$
3) Peak load current [practical]	$I_m = \frac{V_m}{R_f + R_L}$	$I_m = \frac{V_m}{R_f + R_L}$	$I_m = \frac{V_m}{2R_f + R_L}$
4) DC load current	$I_{dc} = \frac{I_m}{\pi}$ $I_{dc} = \frac{V_m}{(R_f + R_L) \cdot \pi}$	$I_{dc} = \frac{2 I_m}{\pi}$ $I_{dc} = \frac{2 \cdot V_m}{(R_f + R_L) \cdot \pi}$	$I_m = \frac{2 I_m}{\pi}$ $I_{dc} = \frac{2 \cdot V_m}{(2R_f + R_L) \cdot \pi}$
5) RMS load current & AC load current	$I_{RMS} = \frac{I_m}{2}$	$I_{RMS} = \frac{I_m}{\sqrt{2}}$	$I_{RMS} = \frac{I_m}{\sqrt{2}}$
6) AC i/p power (ideal)	$P_{ac} = I_{RMS}^2 \cdot R_L$	$P_{ac} = I_{RMS}^2 \cdot R_L$	$P_{ac} = I_{RMS}^2 \cdot R_L$

7) AC i/p power [practical]	$P_{ac} = I_{rms}^2 \cdot (R_L + R_f)$	$P_{ac} = I_{rms}^2 \cdot (R_L + R_f)$	$P_{ac} = I_{Rms}^2 \cdot (2R_f + R_L)$
8) Percentage Regulation	% Regulation $= \frac{R_f}{R_L} \times 100$	% Regulation $= \frac{R_f}{R_L} \times 100$	% Regulation $= \frac{2R_f}{R_L} \times 100$
9) Rms load voltage	$V_{RMS} = \frac{V_m}{2}$	$V_{RMS} = \frac{V_m}{\sqrt{2}}$	$V_{RMS} = \frac{V_m}{\sqrt{2}}$
10) D/p dc-power	$P_{dc} = I_{dc}^2 \cdot R_L$	$P_{dc} = I_{dc}^2 \cdot R_L$	$P_{dc} = I_{dc}^2 \cdot R_L$
11) PIV [peak Inverse v/g]	$PIV = V_m$	$PIV = 2V_m$	$PIV = V_m$
12) Ripple frequency [O/p frequency]	f_{in}	$2f_{in}$	$2 \times f_{in}$
13) Ripple factor	$\gamma = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1}$	$\sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1} = \gamma$	$\gamma = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1}$
	$\gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$	$\gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$	$\gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$

Problems:

1) In a full wave bridge rectifier, the transformer secondary voltage is $100\sin\omega t$. The forward resistance of each diode is 25Ω and the load resistance is 950Ω. Calculate 1) D.C o/p v/g 2) ripple factor 3) Efficiency of rectification 4) PIV

Soln: Given: $V_s = 100\sin\omega t$, $R_f = 25\Omega$, $R_L = 950\Omega$

$V_s = V_2 = V_m \sin\omega t \Rightarrow V_m = 100.$

$$I_m = \frac{V_m}{2R_f + R_L} = \frac{100}{(2 \times 25) + 950} = 0.1A.$$

$$I_{dc} = \frac{2I_m}{\pi} = \frac{2 \times 0.1}{\pi} = 0.063A.$$

1) $V_{dc} = I_{dc} R_L = 0.063 \times 950 = 59.85V$

2) $\gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} = \sqrt{\left(\frac{0.0707}{0.063}\right)^2 - 1}$

$I_{rms} = \frac{I_m}{\sqrt{2}}$

$= \frac{0.1}{\sqrt{2}} = 0.0707A$

$\boxed{\gamma = 0.048}$

3) $P_{dc} = I_{dc}^2 \cdot R_L$

$= (0.063)^2 \times 950$

$P_{dc} = 3.85W$

$P_{ac} = (I_{rms})^2 (2R_f + R_L)$

$= (0.0707)^2 (2 \times 25 + 950)$

$P_{ac} = 5W$

$\% \eta = \frac{P_{ac}}{P_{dc}} \times 100$

$= \frac{5}{3.85} \times 100$

$\boxed{\% \eta = 77.1\%}$

4) $\boxed{PIV = V_m = 100}$

6) In a two diode FWR ckt. the voltage across each half of the transformer secondary is 100V. The load resistance is 950Ω and each diode has a forward resistance of 50Ω. Find the load current and the rms value of the input current.

Soln: Given : $V_s = 100$, $R_f = 50\Omega$, $R_L = 950\Omega$

* $V_m = \sqrt{2} \times V_s = \sqrt{2} \times 100 = 141.42V$
* $I_m = \frac{V_m}{R_f + R_L} = \frac{141.42}{950+50} = 0.141A.$
* $I_{rms} = \frac{I_m}{\sqrt{2}} = \frac{0.141}{\sqrt{2}} = 0.0997A.$
* $I_{dc} = \frac{2I_m}{\pi} = \frac{2 \times 0.141}{\pi} = 0.090A.$

3) A Bridge rectifier is driving a load resistance of 100Ω. It is driven by a source voltage of 230V 50Hz. Neglecting diode resistance. Calculate
1) Average DC voltage 2) Average direct current
3) Frequency of o/p waveform

Soln: Given: $R_L = 100\Omega$, $V_S = 230V$, $f_{in} = 50Hz$.

$V_m = \sqrt{2} \times V_S = \sqrt{2} \times 230 = 325V$

1) $V_{dc} = \frac{2V_m}{\pi} = \frac{2 \times 325}{\pi} = 206.9V$ $\boxed{V_{dc} = 206.9V}$

2) $I_{dc} = \frac{2I_m}{\pi} = \frac{2 \times 3.25}{\pi} = 2.06A$ $\boxed{I_{dc} = 2.06A}$

$I_m = \frac{V_m}{R_L} = \frac{325}{100} = 3.25$

3) o/p frequency $= 2f_{in} = 2 \times 50 = 100Hz$.

4) In a full wave rectifier, the input is from 30-0-30V transformer. The load and diode forward resistance are 100Ω & 10Ω respectively. Calculate the average v/g. rectification efficiency and percentage regulation.

Soln: Given: $V_S = 30V$, $R_L = 100\Omega$, $R_f = 10\Omega$

* $V_m = \sqrt{2} \times V_S = \sqrt{2} \times 30 = 42.426V$.

* $I_m = \frac{V_m}{R_f + R_L} = \frac{42.426}{(100+10)} = 0.3856A$.

* $I_{dc} = \frac{2I_m}{\pi} = \frac{2 \times 0.3856}{\pi} = 0.2455A$

* $V_{dc} = I_{dc} R_L = 0.2455 \times 100 = 24.55V$

* $P_{dc} = (I_{dc})^2 R_L = (0.2455)^2 \times 100 = 6.027\,W$

* $P_{ac} = I_{rms}^2 (R_L + R_f) = (0.272)^2 (10+100) = 8.177\,W$

* $I_{rms} = \frac{I_m}{\sqrt{2}} = \frac{0.3856}{\sqrt{2}} = 0.272\,A.$

* $\%\eta = \frac{P_{dc}}{P_{ac}} \times 100$

$= \frac{6.027\,W}{8.177} \times 100$ $\boxed{\eta\% = 73.61}$

% Regulation $= \frac{R_f}{R_L} \times 100 = \frac{10}{100} \times 100 = 10.$

5) A diode with $V_f = 0.7\,V$ is connected as a half wave rectifier. The load resistance is 600Ω and the (rms) ac i/p voltage is 24V. Determine the peak o/p vlg the peak load current and the diode peak reverse voltage.

Soln: Given: $V_f = 0.7V$. $R_L = 600$. $V_s = 24V$.

* $V_m = \sqrt{2} \times V_s = \sqrt{2} \times 24 = 33.941\,V.$

* $I_m = \frac{V_m - V_f}{R_L} = \frac{33.941 - 0.7\,V}{600} = 55.4018\,mA.$

* $PIV = V_m = 33.941V.$

* Peak o/p voltage $= V_0 = I_m R_L = 55.401 \times 10^{-3} \times 600$

$\boxed{V_0 = 33.24V}$

(or)

$V_0 = V_m - V_f = 33.941 - 0.7 = 33.24V.$

6) The input to a half wave rectifier is $V = 200 \sin 50t$ If $R_L = 1K$ and forward resistance of the diode is 500hms find

1) dc current through the diode
2) a.c & r.m.s value of the current through the ckt.
3) The d.c o/p v/g.
4) The a.c i/p power
5) d.c power o/p
6) Rectifier efficiency.

Soln: Given : $V_i = 200 \sin 50t$, $R_L = 1K$, $R_f = 500\Omega$

$V_i = V_m \sin \omega t$

$\boxed{V_m = 200}$

Peak value of load current, $I_m = \frac{V_m}{R_f + R_L} = \frac{200}{50 + 1K}$

$I_m = 0.19$

$\boxed{I_m = 190\,mA}$

1) $I_{dc} = \frac{I_m}{\pi} = \frac{190 \times 10^{-3}}{\pi}$

$\boxed{I_{dc} = 60mA}$

2) $I_{RMS} = \frac{I_m}{2} = \frac{190}{2} = 95mA$

3) D.C o/p v/g $= I_{dc} \times R_L$
$= 60mA \times 1K$

$\boxed{V_{dc} = 60 \text{ volts}}$

5) $P_{dc} = (I_{dc})^2 \times R_L$
$= (0.06)^2 \times 1000$

$\boxed{P_{dc} = 3.6W}$

4) A.C i/p power, P_{ac}

$P_{ac} = (I_{RMS})^2 \times (R_L + R_f)$
$= (0.095)^2 \times (1K + 50)$

$\boxed{P_{ac} = 9.476W}$

6) % efficiency $= \frac{P_{dc}}{P_{ac}} \times 100$

$= \frac{3.6}{9.476} \times 100$

$\boxed{\%\eta = 37.9}$

7) An a.c vlg of 25V is applied in series with a silicon diode and a load resistance of 1000Ω. If the forward resistance of the diode is 10Ω. Find the peak current through the diode and peak o/p vlg.

Soln: Given: $V_{rms} = 25V$, $R_L = 1000\Omega$ $R_f = 10\Omega$

$$V_m = \sqrt{2} \times V_{rms} = 1.414 \times 25 = 35.35V.$$

Peak value of the current, $I_m = \frac{V_m}{R_f + R_L}$

$$= \frac{35.35}{10 + 1000} = 35mA.$$

$$V_{dc} = I_{dc} \cdot R_L = \frac{I_m}{\pi} \cdot R_L = \frac{0.035}{\pi} \times 1000$$

$$\boxed{V_{dc} = 11.14V}$$

Peak o/p voltage $= I_m \times R_L = 0.035 \times 1000$

$$\boxed{V_m = 35V.}$$

8) A full wave rectifier with transformer ratio 230V, 50-0-50V has a load resistance R_L of 1KΩ. If diode forward resistance $R_f = 20\Omega$. Find 1) the maximum value of current in the diodes when conducting.
2) Dc value of current through R_L 3) o/p dc vlg.
4) peak Inverse voltage

Soln: Given: $V_S = 50V$, $R_L = 1K$, $R_f = 20\Omega$

The a.c & rms value of a.c vlg across each secondary half is 50V.

$$\therefore V_m = \sqrt{2} \times 50 = 70.7V.$$

1) $I_m = \frac{V_m}{R_f + R_L} = \frac{70.7}{20+1000} = 69.3\,mA$

2) I_{dc}, dc value of current through $R_L = \frac{2I_m}{\pi}$

$$\boxed{I_{dc} = 44.12\,mA}$$

3) o/p. dc vlg across $R_L = I_{dc} \times R_L$

$= 44.12\,mA \times 1K$

$$\boxed{V_{dc} = 44.12\ volts}$$

4) Peak Inverse voltage, $PIV = 2V_m$

$= 2 \times 70.7$

$$\boxed{PIV = 141.4V}$$

5) A bridge type full wave rectifier uses four diodes and transformer of ratio 230V:110V the forward resistance of each diode is 25Ω and a reverse resistance is ∞. If the load is a pure resistance of 500Ω. Find

1) maximum value of current in the circuit
2) D.C value of current through R_L
3) D.C value of vlg across R_L
4) PIV across non-conducting diodes.

Soln: Given: $V_2 = 110V$, $R_f = 25\Omega$, $R_L = 500\Omega$

Rms value of vlg. $V_m = \sqrt{2} \times 110 = 155.56V$.

1) $I_m = \frac{V_m}{2R_f + R_L} = \frac{155.56}{[2 \times 25 + 500]} = 282.8\,mA$

2) Dc value of current through R_L.

$$I_{dc} = \frac{2I_m}{\pi} = \frac{2 \times 282.8 \times 10^{-3}}{\pi} = 180\,mA.$$

a) $V_{dc} = I_{dc} \times R_L = (180 \times 10^{-3}) \times 500$

$$\boxed{V_{dc} = 90V}$$

b) PIV across non-conducting diodes $= V_m = 155.56$ V.

10). A HWR DC output V/g at no load is found to be 12V, when full load current of 0.4A is drawn from it the voltage is found to be 10V. Find the % of voltage regulation.

Soln: Given: $V_{NL} = 12V$. $V_{FL} = 10$ V.

$$\% \text{ Regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100$$

$$= \frac{12 - 10}{10} \times 100$$

$$= 20\%$$

11). For a Sinusoidal eq 100 Sin 210t volts is applied to Full wave bridge rectifier. Determine the efficiency if $R_L = 1000\Omega$ and $R_L = 2K\Omega$. Consider diodes with forward resistance $R_f = 10\Omega$ are used.

Soln: Given: $V_s = 100 \text{ Sin } 210t$ $R_f = 10.1\Omega$ $V_m = 100$ V.

Case i) $R_L = 1000\Omega$

$$\eta = \frac{0.812}{\left[\frac{2R_f}{R_L} + 1\right]} \times 100\%$$

$$\eta = \frac{0.812}{\left[\frac{2 \times 10}{1000} + 1\right]} \times 100 = 79.6\%$$

Case ii) $R_L = 2000\Omega$

$$\eta = \frac{0.812}{\left[\frac{2R_f}{R_L} + 1\right]} = 80.39\%$$

FILTERS

The main function of a filter is to reduce & eliminate noise from the information. In the rectifier circuit it is used to minimize the ripple content in the rectified o/p.

Need: The o/p of the rectifier circuit is pulsating DC. Such an o/p has a d.c components and some a.c components called ripples. such an output is not of much use for driving sophisticated electronic devices and circuits. which requires a very steady dc o/p, which should be almost as smooth as the dp from a battery. such an o/p may be obtained by introducing filter.

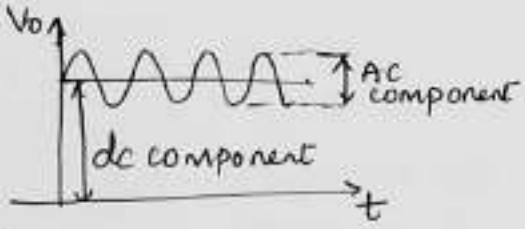


fig: o/p from rectifier.

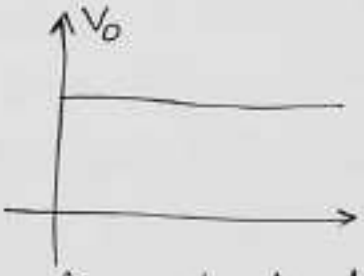
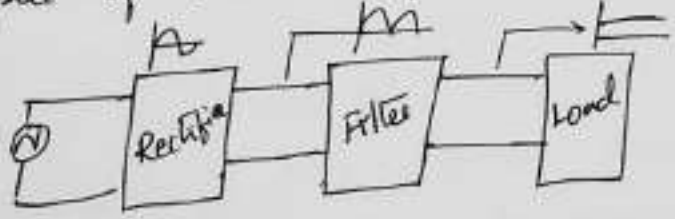


fig: steady dc o/p.

Definition: The filter may be defined as. it is a device, which removes AC component of the rectifier output but allows the DC component to reach the load & it is a circuit, which converts pulsating output of the rectifier into a steady DC level.



Filters should be installed blw the rectifier blw the rectifier and the load as shown in fig above

Types of filters:

1) Capacitor
2) Inductor
3) LC-filter
4) CLC filter & π section

Out of all these four types of filters, capacitor filter is most commonly used because of its low cost

Capacitor Filter:

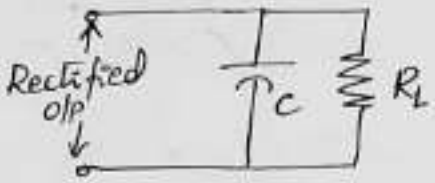


fig: ckt of a capacitor filter

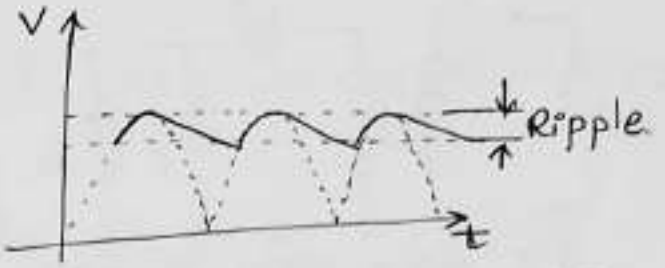


fig: o/p of the Rectifier with capacitor.

The filter consists of a capacitor C connected in parallel with load resistance R_L. The o/p is available across the load resistor. The o/p waveform shows that the ripple is reduced to a great extent due to the addition of capacitor.

We know that capacitor store energy. They can take a charge and then later delivers that charge to the load. With the increase in rectifier v/g, the capacitor is charged and rate current is supplied to the load later when the rectifier o/p decreases the capacitor discharges through the load and the v/g across the parallel combination of R and C decreases. This decrease is only slight because the next v/g peak comes immediately and charges the capacitor. This process is repeated again and again. and hence the ripple is reduced

The factors which determines the effectiveness of capacitor are

1) Size of the capacitor
2) The value of the load
3) The time bw the pulsations.

Rectifier With Capacitor Filter

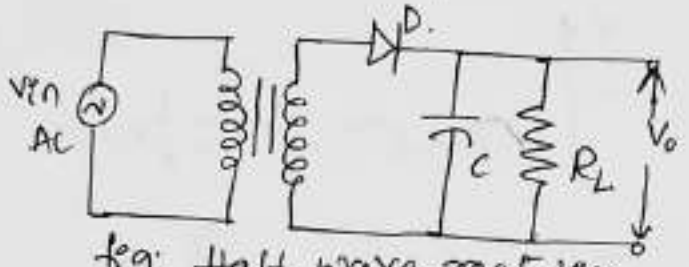
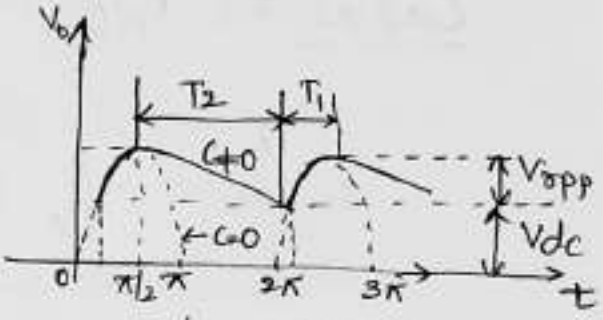


fig: Half wave rectifier.



o/p waveform.

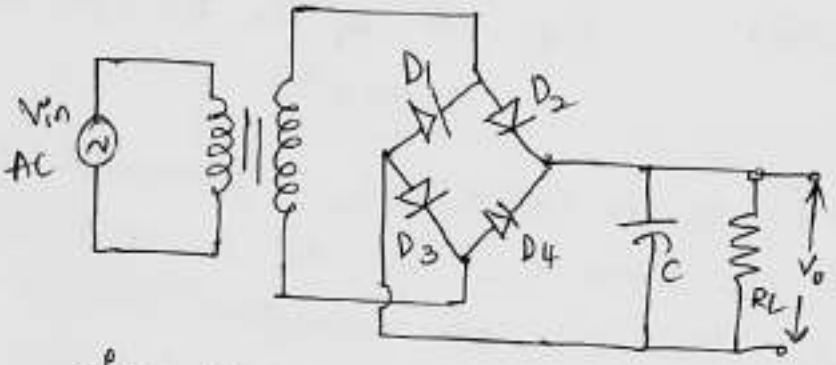
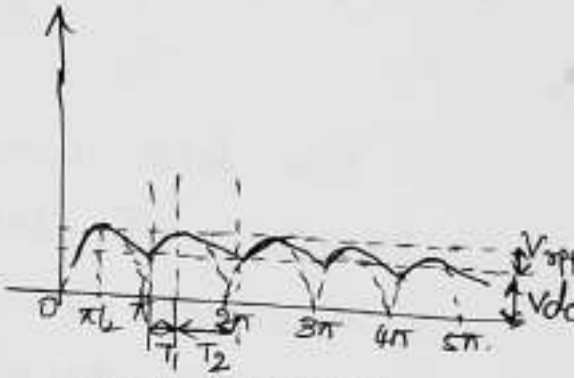


fig: Full wave rectifier.



o/p waveform

The capacitor in both the circuits are placed across the rectifier o/p R_L i.e Load. The pulsating DC of the rectifier is applied across the capacitor. As rectifier voltage increases it charges the capacitor towards V_m because initially capacitor acts as a short. At the end of quarter cycle ($\pi/2$) it is charged to peak value V_m of the rectifier v/g as shown in fig above. Once capacitor voltage reaches V_m diode is reverse biased where anode of diode is positive but less than V_m hence diode is reverse biased and stops conducting. Now capacitor

discharges through the load and the voltage across it decreases. Capacitor discharges until the input voltage is less than capacitor voltage. Once the input voltage is greater than capacitor voltage the diode is forward biased and capacitor charges to V_m. and same cycle repeats.

The expression for ripple factor (γ) is given by.

$$\gamma = \frac{1}{2\sqrt{3} f C \cdot R_L} \rightarrow \text{for Half wave rectifier}$$

$$\gamma = \frac{1}{4\sqrt{3} R_L \cdot f \cdot C} \rightarrow \text{for full wave rectifier.}$$

where,

$f \rightarrow$ Frequency $\quad R_L \rightarrow$ Load resistance

$C \rightarrow$ Capacitance

DC output voltage

$$V_{dc} = V_m - \frac{V_{rpp}}{2}$$

$$V_{dc} = V_m - \frac{I_{dc}}{2fC} \qquad I_{dc} = \frac{V_{dc}}{R_L}$$

$$V_{dc} = V_m - \frac{V_{dc}}{2f R_L C}$$

$$\& \quad \boxed{V_{dc} = \frac{V_m}{1 + \frac{1}{2f R_L C}}} \rightarrow \text{for Half wave rectifier}$$

for full wave rectifier.

$$V_{dc} = V_m - \frac{I_{dc}}{4fC}$$

$$\boxed{V_{dc} = \frac{V_m}{1 + \frac{1}{4f R_L C}}}$$

Problems:

1) A full wave rectifier using centre tapped transformer supplies a resistive load of 1KΩ. The transformer secondary end to end voltage is 60V rms at 50Hz. The filter capacitance is 500μF. Calculate

a) Ripple factor b) output resistance of the filter (R_0)

c) V_{dc} d) I_{dc} e) % regulation.

Soln: Given: $R_L = 1K$, $C = 500\mu F$. $V_{rms} = 60V$. [end to end].

$\therefore V_{rms} = 30V$.

a) $$\gamma = \frac{1}{4\sqrt{3}\, R_L \cdot C \cdot f} = \frac{1}{4\sqrt{3} \times 1 \times 10^3 \times 500 \times 10^{-6} \times 50}$$

$$\boxed{\gamma = 0.0058}$$

b) O/p resistance of the filter R_0

$$R_0 = \frac{1}{4fC} = \frac{1}{4 \times 50 \times 500 \times 10^{-6}} = 10\Omega$$

c) $$V_{dc} = \frac{V_m}{1 + R_0/R_L} = \frac{42.42}{1 + 10/1K} = 42V$$

$$V_m = \sqrt{2} \times V_{rms} = \sqrt{2} \times 30 = 42.42V$$

d) $$I_{dc} = \frac{V_{dc}}{R_L} = \frac{42V}{1K}$$

$$\boxed{I_{dc} = 42mA}$$

e) % Regulation $= \frac{R_0}{R_L} \times 100\%$

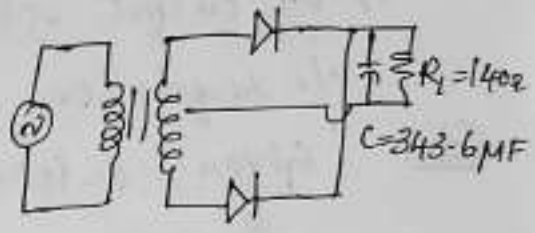
$$= \frac{10}{1 \times 10^3} \times 100$$

$$= 1\%$$

2) Design a full wave rectifier with C-filter for the following specifications: Ripple factor < 0.06. o/p dc vlg = 35V, Maximum load current = 250mA.

Soln: Given: $V_{dc} = 35V$, $I_{dc} = 250mA$, $\gamma = 0.06$

Assuming, $f = 50Hz$



$$R_L = \frac{V_{dc}}{I_{dc}} = \frac{35V}{250mA} = 140\Omega$$

$$\gamma = \frac{1}{4\sqrt{3} f C R_L}$$

$$C = \frac{1}{4\sqrt{3} f \gamma R_L} = \frac{1}{4\sqrt{3} \times 50 \times 140 \times 0.06} = 343.66\mu F.$$

$$V_m = V_{dc} + \frac{I_{dc}}{4fC}$$

$$= 35 + \frac{250mA}{4 \times 50 \times 343.66 \times 10^{-6}} = 38.53V$$

$$V_m = \sqrt{2} V_{rms}$$

$$V_m = \frac{V_m}{\sqrt{2}} = \frac{38.53V}{\sqrt{2}} = 27.3V$$

3) A full wave bridge rectifier is supplied from the transformer secondary voltage of 100V. Calculate the dc o/p voltage and peak Inverse voltage of the diode employed.

Soln: Given: $V_{(rms)} = 100V$, $V_{dc} = ?$, $PIV = ?$

* $V_m = \sqrt{2} \cdot V_{rms} = \sqrt{2} \times 100$

$\boxed{V_m = 141.42V}$

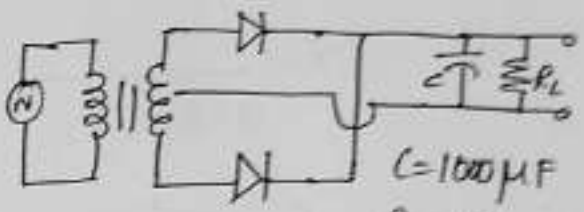
* $PIV = V_m$

$\boxed{PIV = 141.42V}$

* $V_{dc} = \frac{2V_m}{\pi} = \frac{2 \times 141.42}{\pi} = 90V.$

4) Draw the circuit diagram of a full wave rectifier with capacitor filter. The circuit uses a capacitor of 1000μF and provides a dc load current of 500mA at 2% ripple. Assume f = 50Hz. Calculate:
1) D.C output voltage 2) peak rectified voltage and
3) % regulation.

Soln: Given: $C = 1000\mu F$, $I_{dc} = I_L = 500mA$, $\gamma = 0.02$, $f = 50Hz$



$$\gamma = \frac{1}{4\sqrt{3}R_L Cf}$$

$$R_L = \frac{1}{4\sqrt{3}fC\gamma} = \frac{1}{4\sqrt{3}\times 50\times 1000\times 10^{-6}\times 0.02}$$

$$\boxed{R_L = 144.34\Omega}$$

i) DC o/p Vlg.

$$V_{dc} = I_{dc} R_L = 500\times 10^{-3}\times 144.34\Omega$$

$$\boxed{V_{dc} = 72.17V}$$

ii) $V_m = V_{dc} + \frac{I_{dc}}{4fC}$ & $V_m = V_{dc}\left[1 + \frac{R_0}{R_L}\right]$

$$V_m = 72.17 + \frac{500\times 10^{-3}}{4\times 50\times 1000\times 10^{-6}} \qquad R_0 = \frac{1}{4fC} = 5\Omega$$

$$\boxed{V_m = 74.67V} \qquad \boxed{V_m = 74.67V}$$

iii) % Regulation $= \frac{R_0}{R_L}\times 100 = \frac{5\Omega}{144.34}\times 100$

$$\boxed{\%\text{ Regulation} = 3.64\%}$$

5) Design a FWR with a capacitor filter to meet the following specifications. DC o/p vlg = 15V, R_L = 1K, RMS ripple vlg on capacitor < 1% of DC o/p vlg.

Soln: Given: $V_{dc} = 15V$, $R_L = 1K$, $\gamma = 0.01$, $f = 50Hz$,

$V_{r(rms)}$ = 1% of 15V

$= 0.01 \times 15$

$\boxed{V_{r(rms)} = 0.15V}$ → This is the rms value of the ripple voltage

$$\gamma = \frac{1}{4\sqrt{3} f C R_L}$$

$$C = \frac{1}{4\sqrt{3} f R_L \gamma} = \frac{1}{4\sqrt{3} \times 50 \times 1 \times 10^3 \times 0.01}$$

$\boxed{C = 288.675\mu F}$

$$V_{dc} = V_m - I_{dc}\left[\frac{1}{4fC}\right]$$

$$I_{dc} = \frac{V_{dc}}{R_L} = \frac{15V}{1K}$$

$\boxed{I_{dc} = 15mA}$

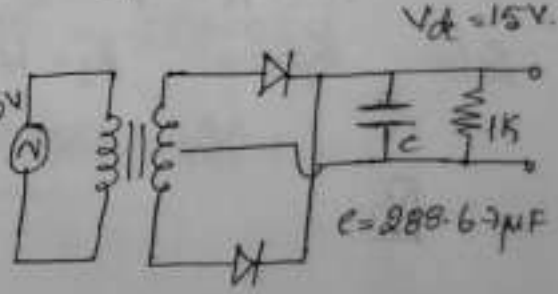
$$V_m = V_{dc} + I_{dc}\left[\frac{1}{4fC}\right]$$

$$= 15 + 15 \times 10^{-3}\left[\frac{1}{4 \times 50 \times 288.6 \times 10^{-6}}\right]$$

$\boxed{V_m = 15.25V}$

$$V_{rms} = \frac{V_m}{\sqrt{2}} = \frac{15.25}{\sqrt{2}} = 10.31V$$

$\boxed{V_{rms} = 10.31V}$



6) In a FWR with a capacitor filter, the load current from the circuit operating from 230V, 50Hz supply is 10mA. Estimate the value of capacitor required to keep the ripple factor less than 1%.

Given: $I_L = 10mA$, $V_{dc} = 230V$, $f = 50Hz$, $\gamma = 0.01 = 1\%$

$$V_m = \sqrt{2} \times 230 = 325.269V$$

$$R_L = \frac{V_{dc}}{I_L} = \frac{207.07}{10 \times 10^{-3}} = 20.70K$$

$$V_{dc} = \frac{2V_m}{\pi} = \frac{2 \times 325.269}{\pi} = 207.07V$$

$$\gamma = \frac{1}{4\sqrt{3} R_L f C}$$

$$C = \frac{1}{4\sqrt{3} R_L f \gamma} = \frac{1}{4\sqrt{3} \times 50 \times 20.70 \times 10^3 \times 50 \times 0.01}$$

$$\boxed{C = 13.94\mu F}$$

7) A full wave bridge rectifier supplies a load of 400Ω in parallel with a capacitor of 500μF. If the ac supply voltage is $230V \sin 314t$ find the 1) Ripple factor 2) D.C. load current.

Soln: Given: $R_L = 400\Omega$, $C = 500\mu F$, $V_m \sin\omega t = 230 \sin 314t$

$V_m = 230V$ $\omega = 314$

$2\pi f = 314$

$f = \frac{314}{2\pi} = 50Hz$.

1) $\gamma = \frac{1}{4\sqrt{3} R_L f C} = \frac{1}{4\sqrt{3} \times 400 \times 50 \times 500 \times 10^{-6}}$

$\boxed{\gamma = 0.0144}$

2) $I_{dc} = \frac{2I_m}{\pi} = \frac{2V_m}{\pi R_L} = \frac{2 \times 230}{\pi \times 400}$

$I_{dc} = 0.366A$

$\boxed{I_{dc} = 36.6mA}$

(8) A full wave rectifier has a load of 2KΩ. The AC voltage applied to the diodes is 200-0-200V Assuming Ideal diodes. Calculate

1) Average DC current 2) average DC vlg and

3) Ripple voltage if a C=500μF is connected. what is new ripple?

Soln: Given: $R_L = 2K$, $V_S = 200V$, $f = 50Hz$, $C = 500\mu F$

$V_m = \sqrt{2} \times V_S = \sqrt{2} \times 200 = 282.842V$

1) $I_m = \frac{V_m}{R_L} = \frac{282.84}{2 \times 10^3} = 0.1414A$

$I_{dc} = \frac{2I_m}{\pi} = \frac{2 \times 0.1414}{\pi} = 0.09A$ $\boxed{I_{dc} = 9mA}$

2) $V_{dc} = I_{dc} R_L = 0.09 \times 2 \times 10^3 = 180.03V$

3) $\gamma = \frac{V_{ac}}{V_{dc}}$ w.k.t $\gamma = 0.48$ for F.W.R

$V_{ac} = \gamma V_{dc}$ $\boxed{V_{ac} = 86.4V}$

If a new capacitor filter of C = 500μF is used then,

$$\gamma = \frac{1}{4\sqrt{3} f C R_L} = \frac{1}{4\sqrt{3} \times 50 \times 500 \times 10^{-6} \times 2 \times 10^3}$$

$$\boxed{\gamma = 2.886 \times 10^{-3}}$$

$$\gamma = \frac{V_r(rms)}{V_{dc}}$$

$$V_r(rms) = \gamma \times V_{dc}$$

$$= 2.886 \times 10^{-3} \times 180.03$$

$$\boxed{V_r(rms) = 0.5196 V}$$

(9) In a centre tap full wave rectifier, the forward resistance of the diode is 10Ω, the load resistance is 2K. The vlg across half the secondary winding is 220V. Calculate the ripple factor & efficiency of the rectification. If a capacitor of value 25μF is connected across the load what is the modified ripple factor.

Soln: Given: $R_f = 10\Omega$, $R_L = 2K$, $V_2 = 220$, $C = 25\mu F$.

$$V_m = \sqrt{2} \times V_2 = \sqrt{2} \times 220 = 311.12V$$

$$I_m = \frac{V_m}{R_L + R_f} = \frac{311.12}{10 + 2000} = 0.155A = 155\ mA$$

$\therefore$ DC load current, $I_{dc} = \frac{2I_m}{\pi} = \frac{2 \times 155 \times 10^{-3}}{\pi} = 0.09867$

$= 98.6mA$

RMS value of load current. $I_{rms} = \frac{I_m}{\sqrt{2}} = 109.6\,mA.$

$$\gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{109.6\times10^{-3}}{98.6\times10^{-3}}\right)^2 - 1} \quad = 0.4853$$

$\boxed{\gamma = 48.5\,\%}$ → without capacitor filter

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{I_{dc}^2 \cdot R_L}{(I_{rms})^2 (R_L + R_f)} = \frac{(98.6\times10^{-3})^2 \times 2\times10^3}{(109.6\times10^{-3})^2 (2K+10)}$$

$$= \frac{19.44}{24.144}$$

$\boxed{\eta = 80.5\,\%}$

$$\gamma = \frac{1}{4\sqrt{3} R_L f C} = \frac{1}{4\sqrt{3}\times2\times10^3\times50\times25\times10^{-6}} = 0.0577.$$

$\boxed{\gamma = 5.7\,\%}$ → with capacitor filter

(10) In a HWR circuit, fed from 230V, it is desired to have a ripple factor $\gamma \le 0.005$. Estimate the value of the capacitance needed if $I_L = 0.5A$. Turns ratio is 4.6.

Soln: Given: $I_L = 0.5A$, $\gamma \le 0.005$, $V_1 = 230V$, $\frac{N_1}{N_2} = 4.6$

$$\frac{V_2}{V_1} = \frac{N_2}{N_1}$$

$\because V_1$ = primary voltage V_2 = secondary voltage

$$\frac{V_2}{V_1} = \frac{1}{4.6} \Rightarrow V_2 = \frac{230}{4.6} = 50V.$$

$V_m = \sqrt{2} \times 50 = 70.7\ V.$

$$R_L = \frac{V_{dc}}{I_L} = \frac{70.7}{0.5} = 141.4\ \Omega$$

$$\gamma = \frac{1}{2\sqrt{3} \cdot f \cdot C \cdot R_L}$$

$$C = \frac{1}{2\sqrt{3} \times 50 \times \gamma \times 141.4}$$

$$= \frac{1}{2\sqrt{3} \times 50 \times 0.005 \times 141.4}$$

$$\boxed{C = 8169\ \mu F}$$

(11) A FWR has $R_L = 10K\Omega$ and a capacitive filter having capacitance of $C = 20\mu F$. The applied voltage is $V = 50 \sin 2\pi 50t$ Calculate its ripple factor.

Soln: Given: $R_L = 10K$, $C = 20\mu F$,

$V = 50 \sin 2\pi 50t \Rightarrow V_m \sin 2\pi ft$.

$V_m = 50 \quad f = 50\ Hz.$

$$\gamma = \frac{1}{4\sqrt{3} \times 50 \times 20 \times 10^{-6} \times 10 \times 10^{3}}$$

$$\boxed{\gamma = 0.00144}$$

(12) A half wave rectifier uses a transformer with turns ratio 2:1. The load resistance is 500Ω. If the primary voltage is 540V, 50Hz. Calculate

a) the peak inverse voltage

b) the dc output voltage. Neglect cut-in voltage and forward resistance of the diode.

Soln: Given: $N_1 : N_2 = 2:1$, $R_L = 500\Omega$, $R_f = 0$

$$\frac{N_1}{N_2} = \frac{2}{1} = \frac{V_1}{V_2} = \frac{540}{V_2}$$

Secondary vlg. $V_2 = \frac{540}{2} = 270$.

$\therefore$ peak vlg $V_m = \sqrt{2} \times 270 = 381.8$

a) Peak Inverse voltage. PIV $= V_m = 381.8$.

b) Peak current

$$I_m = \frac{V_m}{R_L} = \frac{381.8}{500} = 763.6\,mA.$$

DC o/p current

$$I_{dc} = \frac{I_m}{\pi} = \frac{763.6 \times 10^{-3}}{\pi} = 243\,mA.$$

DC o/p vlg

$$V_{dc} = I_{dc} \cdot R_L$$
$$= (243 \times 10^{-3}) \times 500$$

$$\boxed{V_{dc} = 121\,V.}$$

(13) Ideal diodes are used in a bridge rectifier with a source of 230V, 50Hz across the primary of the transformer If the load resistor is 200Ω and turns ratio of transformer is 6:1, find the dc o/p voltage and frequency of the o/p

Soln: Given: $V_p = 230V$, $f = 50Hz$, $R_L = 200\Omega$, $N_1 : N_2 = 6:1$

RMS vlg across the secondary of the transformer $= \frac{N_2}{N_1} \cdot V_p$

$$= \frac{1}{6} \times 230 = 38.3V.$$

$\therefore$ Maximum vlg across the secondary of the transformer

$$V_m = \sqrt{2} \times 38.3 = 54.2V.$$

$\therefore$ dc o/p vlg. $V_{dc} = \frac{2V_m}{\pi} = \frac{2 \times 54.2}{\pi} = \underline{34.5\,V}$.

$\therefore$ fout $= 2f_{in} = 2 \times 50 = \underline{100Hz}$.

(14) A bridge rectifier has 4 identical diodes of forward resistance of 5Ω each. It is applied from a transformer with output voltage of 20V (rms) and secondary winding resistance of 10Ω calculate

i) dc o/p v/g at a d.c load current of 100 mA.

ii) rms value of o/p v/g at a dc load current of 200mA.

iii) rms value of the ac component of the v/g in part (ii).

Soln: Given: $R_s = 10\Omega$, $R_f = 5\Omega$. $V_m = \sqrt{2} \times 20 = 28.28\,V$.

i) $I_{dc} = 100\,mA$.

$$I_{dc} = \frac{2I_m}{\pi} \Rightarrow I_m = \frac{I_{dc} \times \pi}{2}$$

$$I_m = \frac{100 \times 10^{-3} \times \pi}{2}$$

$$\boxed{I_m = 157.08\,mA}$$

Peak current $I_m = \dfrac{V_m}{R_L + 2R_f + R_s}$

$$R_L = \frac{V_m}{I_m} - 2R_f - R_s$$

$$= \frac{28.28}{157.08 \times 10^{-3}} - 2(5) - 10$$

$$\boxed{R_L = 160\Omega}$$

$V_{dc} = I_{dc} \cdot R_L = 100 \times 10^{-3} \times 160 = 16V$

(ii) $I_{dc} = 200\,mA$

$$I_m = \frac{\pi I_{dc}}{2} = 314.16\,mA$$

$$R_L = \frac{V_m}{I_m} - 2R_f - R_s = \frac{28.28}{314.16 \times 10^{-3}} - 2(5) - 10$$

$$\boxed{R_L = 70\Omega}$$

$V_{dc} = 200 \times 10^{-3} \times 70 = 14V$

(iii) $\gamma = \dfrac{V_{o.rms}}{V_{dc}} = 0.483 \Rightarrow V_{o.rms} = \gamma \cdot V_{dc} = 0.483 \times 14 = 6.7\,V$

$$V_{rms} = \sqrt{V_{dc}^2 + V_{o.rms}^2} = 15.5\,V.$$

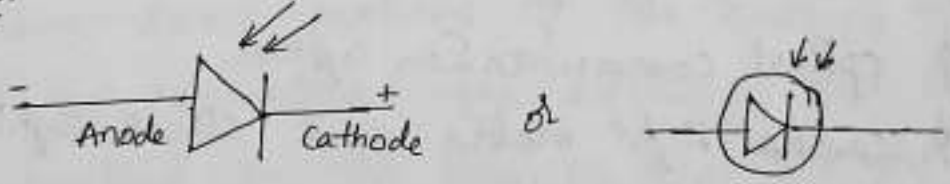
Photo Diode

A photodiode is a PN Junction & PIN semiconductor device which converts a light energy into an electric current. & voltage depends upon the mode of operation.

The current is generated when photons are absorbed in the photodiode. It is also referred as a photo detector & photo sensor. photodiodes are specially designed to operate in reverse bias condition.

The construction of photodiode is similar to the normal PN junction Diode. PIN structure [p-type: intrinsic: N-type] is used instead of PN Junction because PIN structure provides fast response time. This construction technique is called ion implantation, where the surface of layer of N type is bombarded with p type silicon ions to produce p-type layer of 1μm thick. During the formation of the diode, excess electrons move from n-type to p-type and holes from p-type to n-type this process is called diffusion. resulting in Depletion layer

Circuit Symbol:



Working:

The width of the depletion region is more incase of the reverse bias condition. hence photodiode is operated in reverse bias condition. The junction of photodiode is illuminated by the light source. the photons strike the junction surface. The photons impart their energy in the

flow of light to the junction Due to which the covalent bonds present in the depletion region will break into free electrons and holes. These are attracted by the potential across the depletion region which leads to the current called photon current. There is a flow current in the pN junction when there is no light illuminated that current is called Dark current.

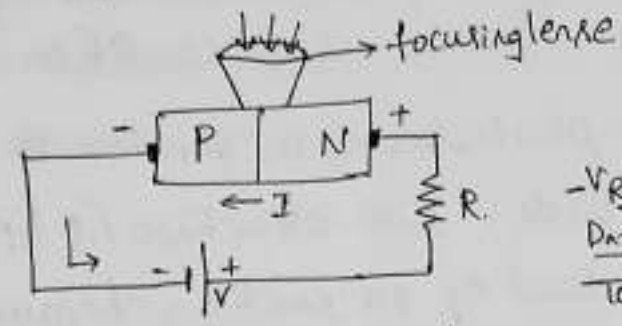


fig: Biasing of photodiode.

The V-I characteristics of photo diode is as shown in fegure.

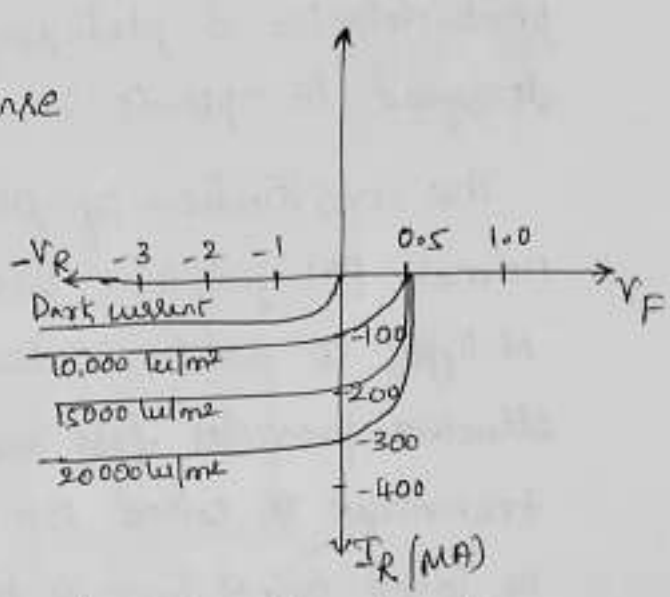


fig: V-I characteristics of photo diode.

Applications:

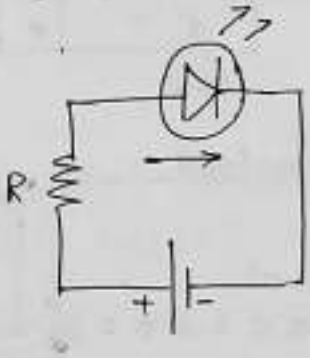
1) photo Diodes are mainly used to measure the intensity of light i.e light meters
2) Solar cell panels
3) optical communication system.
4) camera light meters and street lights.
5) Smoke detectors
6) Burglar alarm.
7) Logic circuits and analyzers
8) consumer devices like CD players, Televisions and remote controls in VCRs.
9) Automotive Devices.

Light Emitting Diode [LED]

LED is a pN-junction Diode which emits light when an electric current passes through it in the forward direction. It is a device which converts Electrical energy into Light energy. This phenomenon is called Electroluminescence.

The Semiconductor material used in LED is Gallium Arsenide [GaAs], Gallium phosphide (GaP) or Gallium Arsenide phosphide [GaAsP].

Symbol:



Working: The charge carriers recombine in a forward biased pN junction as the electrons cross from the N-region and recombine with the holes existing in the p-region. Free electrons are in the conduction band of energy levels. while holes are in the valence band. Thus the energy level of the holes is less than the energy levels of the electrons. some portions of the energy must be dissipated to recombine the electrons and holes. This energy is emitted in the form of heat & light.

The working of the LED depends on the quantum theory. The Quantum theory states that when the electrons decreases from the higher level to lower level, it emits energy in the form of photons. The energy of the photons is equal to gap btw the higher & lower level i.e $\boxed{E = h\nu}$

$E = h\nu$

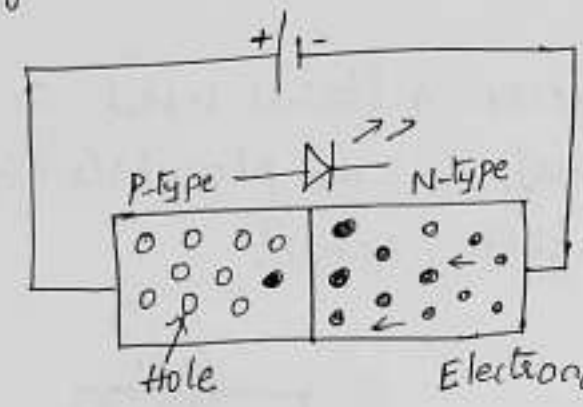
$\boxed{\nu = \frac{E}{h}}$

$h \rightarrow$ plank's constant

$E \rightarrow$ Energy of the photon

$\nu \rightarrow$ frequency of the emitted photon

The above equation shows that the frequency of the emitted light is directly proportional to the Energy gap.



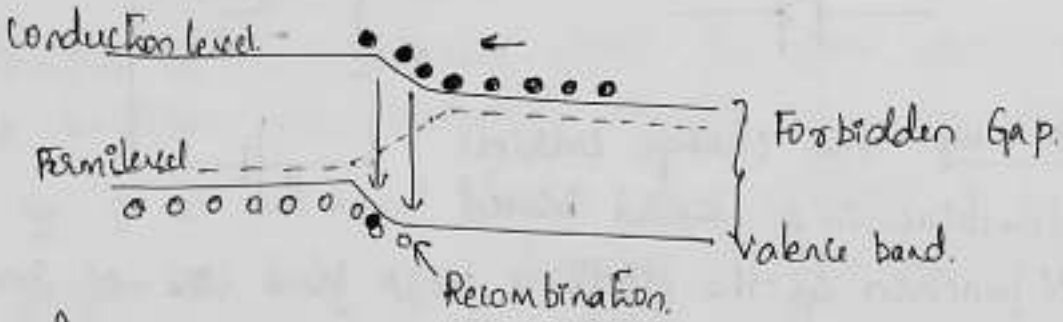


fig: Working of LED

When the junction is reverse biased the LED produces no light. GaAs LEDs emits infrared (IR) radiation which is invisible. GaAsp emits either red & yellow visible light. The colour of the emitted light depends on the band gap of the semiconductor.

Advantages of LED.

1) Lower energy consumption
2) Longer life time
3) improved physical robustness
4) Smaller size
5) faster switching.

Applications:

1) Used in remote control systems such as TV & LCD remote.
2) Used in electronic calculators for showing the digital data
3) Used in traffic signals for controlling the traffic crowds in cities
4) Used in Digital computers for displaying the computer Data
5) Used in Digital watches and automotive heat lamps.
6) Used in medical devices & Camera flashes.

Photo Coupler

photocoupler is a component that transfers electrical signals between two isolated circuits by using light.

It is a packaged device that consists of emitter and a sensor of light that transfers electrical signals b/w two isolated circuits by using light.

photocouplers & optocouplers are used to provide many functions: they can be used to link data across two circuits. they can be used within optical encoders. where the optocoupler provides a means of detecting visible edge transitions on an encoder wheel to detect position

Construction:

All optocouplers consists of two elements: a light source which is almost always a light emitting diode (LED) and a photosensor typically a photoresistor, photodiode photo transistor, silicon-controlled rectifier (SCR) & triac. Both of these elements are seperated by a dielectric (non conducting) barrier.

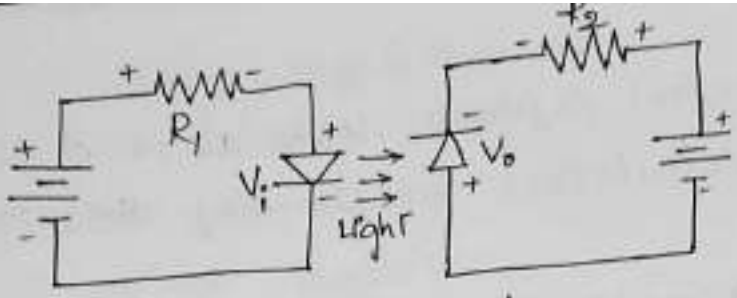


fig: photocoupler.

Working: when input current is applied to the LED. it switches ON and emits infrared light; the photosensor then detects this light and allows current to flow through the output side of the circuit. conversely, when the LED is Off. no current will flow through the photosensor By this method, the two flowing currents are electrically isolated. It consists of LED and photo diode where the circuits are isolated electrically. The above figure shows the basic operation of an optocoupler.

Applications:

1) Input & output switching, especially in electronically noisy environments
2) Switch mode power supplies
3) Signal isolation
4) Power control
5) controlling transistors & triac
6) modern communications.

Voltage Regulators

A voltage regulator is an electronic device & circuit that maintains an essentially constant output voltage for a range of input voltage & load values. It is one part of a d.c power supply.

It is possible to incorporate the complete circuitry of the regulated power supplies on a monolithic silicon chips.

Ic voltage regulators are basically series regulators with all the basic blocks present inside the IC. Therefore it is easier to use Ic voltage regulator instead of discrete voltage regulators.

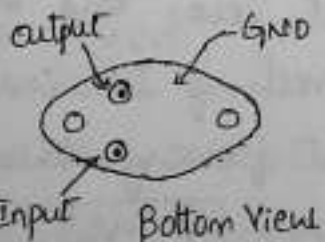
Important features of IC Regulators

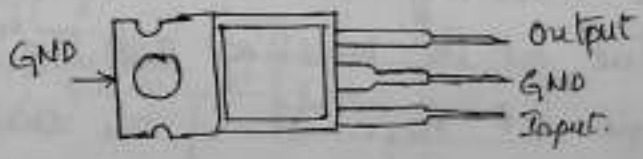
1) Reduction in size
2) Mass production, cost can be reduced.
3) programmable output
4) No external components are required
5) Internally provided short circuit limiting
6) Thermal shutdown.
7) Floating operation facilitate higher voltage
8) output current in excess of 1A.

The IC voltage regulators are classified as follows
1) fixed voltage Regulator 2) Adjustable voltage regulator
3) Switching Regulator.

The IC voltage regulator contains the circuitry for reference source, comparator, amplifier, control device and overload protection all in a single IC. It is available in 2 types of packages.

1) Metal(aluminium) Can package (K package)
2) plastic package (T package).





plastic package

fig: Metal Can package

78xx Series Fixed IC voltage Regulator

The LM78xx series is 3-terminal voltage regulator available in IC form. It is available with several fixed output voltages making them useful in wide range of applications. It is manufactured by National Semiconductor.

In LM 78xx: 78 indicates that op is +ve. and XX = 05, 06, 08, 10, 12, 15, 18, 24

Ex: LM7805 is +5V voltage regulator
7812 is +12V voltage regulator
7824 is +24V voltage regulator.

Block Diagram: The functional block diagram of 78xx series is as shown in figure below.

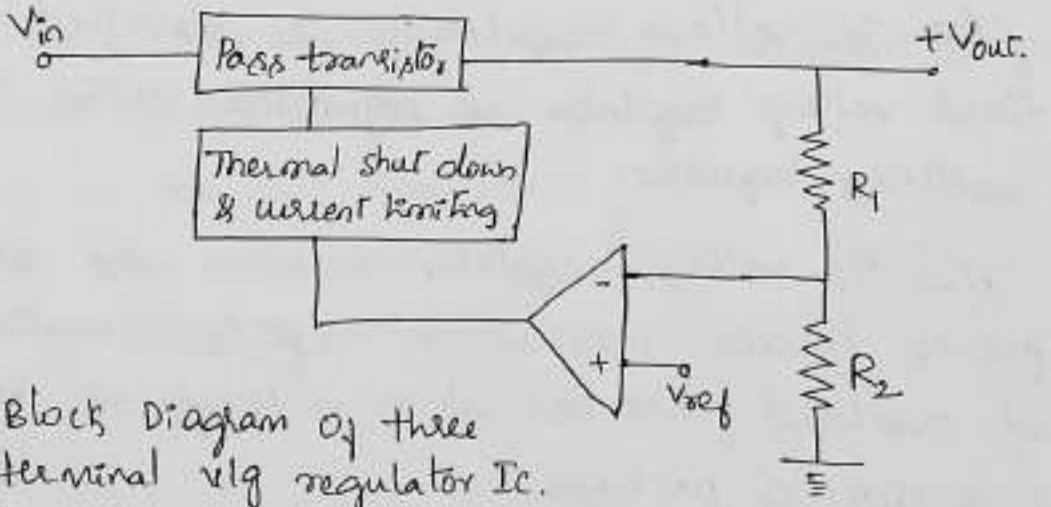


fig: Block Diagram of three terminal vlg regulator IC.

The built-in reference voltage V_{ref} drives the non-inverting input of the operational amplifier. Due to the high gain of the amplifier, the error vlg btw the inverting and non-inverting terminals is almost zero. This makes the value at the inverting and the non-inverting terminal both same i.e V_{ref}. Thus, the current flowing through the potential divider can be written as.

$$I = \frac{V_{ref}}{R_2}$$

The same current flows through the resistor R_1
Thus the output voltage can be given by

$$V_{out} = \left[\frac{V_{ref}}{R_2}\right][R_1 + R_2)$$

The above equation shows that, the output of the regulator can be controlled by putting desired values of R_1 & R_2.

The IC has a series pass transistor that can handle more than 1A of load current provided that adequate heat sinking is used.

It also has thermal shutdown and current limiting options. Thermal shutdown is a feature that will turn off the IC as soon as the internal temperature of the IC rises above its preset value. This rise in temperature may mostly due to external voltage, ambient temperature. The preset cut-off temperature is 175°C.

Due to thermal shutdown and heat sinking. Devices made of 78xx series are more durable. Though these are designed as fixed vlg regulators, can also be used with external components to obtain adjustable voltages and currents.

7805 Fixed IC Voltage Regulator

This is the most commonly used fixed IC vlg regulator. since many of the electronic components require fixed 5V supply.

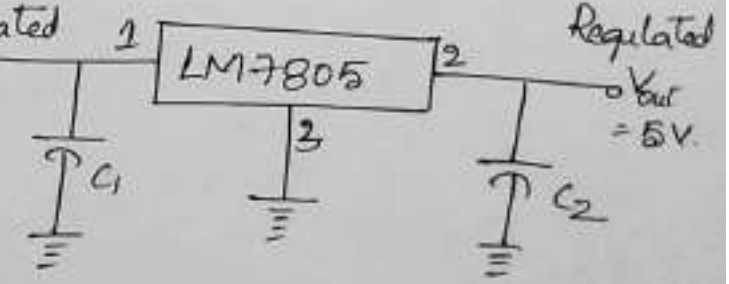


fig shows the connections of 7805 as a fixed vlg regulator.

Pin 1 accepts unregulated input voltage and pin 2 gives regulated output Vlg = 5V, pin 3 is a ground terminal.

A capacitor C_{in} (C_1) is required to cancel out inductive effects. and capacitor C_o [C_2] is to improve the transient response of the regulator and also to reduce noise present at the output. The C_{in} capacitor is connected between the input terminal and the ground terminal. The C_o capacitor is connected blw the ground terminal and the o/p. The typical values of C_1 & C_2 are 0.1 and 1μF respectively.

The difference blw V_{in} & V_{out} [i.e $V_{in} - V_{out}$] is called 'dropout voltage' and it must be typically 2V for 7805.

Module - 2

FET And SCR

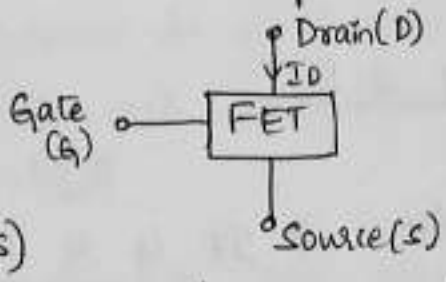
Field Effect Transistor [FET].

FET is a three terminal semiconductor device in which current conduction is by only one type of majority carriers.

* FET is a voltage controlled device where as BJT is a current controlled device. i.e

Drain current in FET is function of i/p v/g where as in BJT o/p current i.e collector current is function of i/p current.

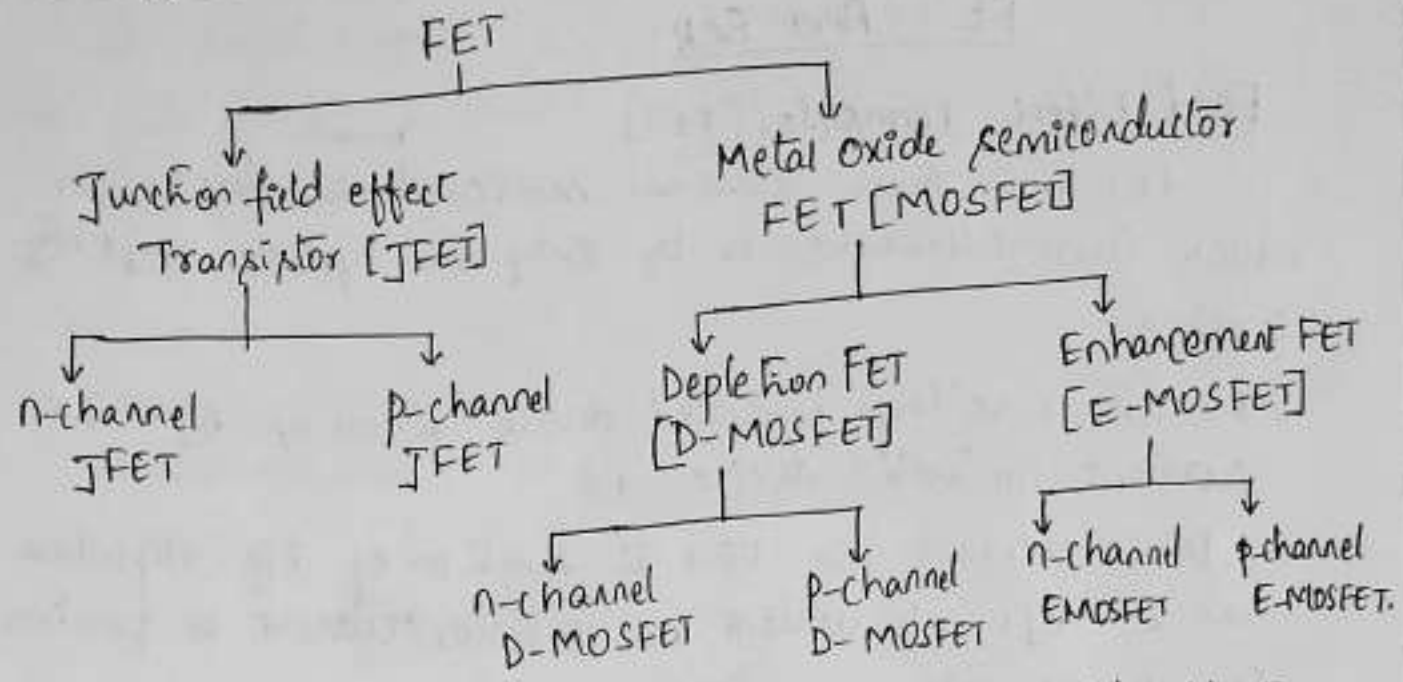
* The three terminals of FET are, Gate, Drain and Source.



$I_D = f(V_{GS})$

* The current conduction is due to the electric field generated by the majority charge carriers hence the name Field effect transistor.
* Unlike BJT, FET requires virtually no input current and gives an extremely high input resistance
* It is called unipolar device: current carried by only one type of charge particles, either electrons or holes. Hence FET is called Unipolar device.
* It requires less space than BJT, hence preferred in ICs.
* FET has very high i/p impedance. Typically in the range of one to several Mega ohms.

Classification:



MOSFET is also called Insulated Gate field effect Transistor [IGFETs].

Comparision b/w FET & BJT

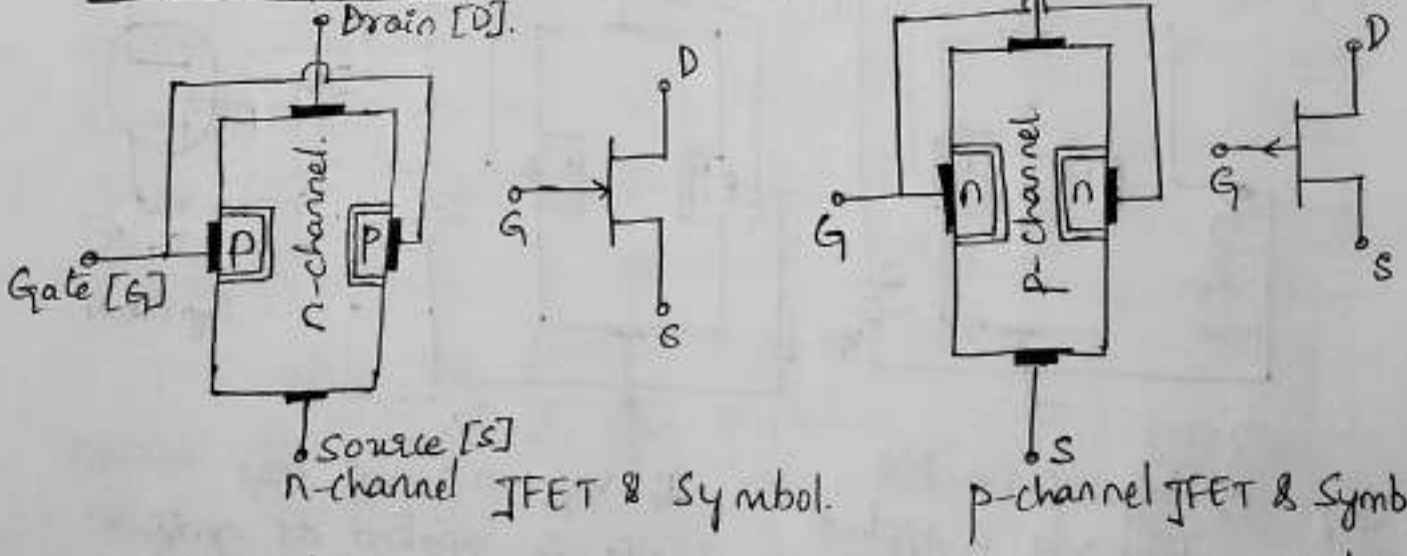
FET	BJT
1). It is a unipolar device	1) It is a bipolar device.
2) It is a v/g controlled device. i/p v/g controls the o/p current	2) It is a current controlled device. o/p current is controlled by i/p current.
3) It exhibits high i/p resistance typically many mega ohms	3) It exhibits low i/p input resistance typically a few kilo ohms.
4) It is less noisy due to carriers crossing single junction	4) It is too noisy due to carriers crossing two junction.
5) It is immune to radiation	5) It is prone to radiation
6) Smaller in size	6) Large in size
7) Thermal stability is High	7) Thermal stability is High.

8) Less sensitive to changes in input signal	8) Highly sensitive to changes in i/p signal.
9) Gain is less in JFET amplifiers. Hence gain B.W product is less	9) Gain is large in BJT amplifiers. Hence gain Bandwidth product is large.
10) It is of two types namely n-channel & p-channel FETs.	10) BJT is also of two types npn transistor and pnp transistors.

The JFET

The JFET [junction field effect transistor] is a type of FET that operates with a reverse biased pn junction to control current in a channel. Depending on the structure JFETs are classified into n-channel and p-channel JFET.

Structure / construction and symbol



n-channel JFET: The structure and the symbol of n-channel JFET is as shown in fig above. The major part of the structure is the n-type material which forms the channel blw the embedded layers of p-type material. It has four ohmic contacts. The wire leads are connected

to each end of the n-channel. The Drain is the upper end and the source is at the lower end. The two p-type regions are diffused into n-type material to form a n-channel. The p-type regions are connected as gate terminal. In the absence of any applied potential the JFET has two p-n junctions under no-bias conditions.

P-channel JFET: In this the major part is p-type material. The two n-type material is diffused into the p-type material to form a p-channel. The two n-type material are connected together to form a gate terminal. The structure and the symbol is as shown in fig.

Operation of n-Channel JFET

Let us consider n-channel JFET biased with V_{DS} [Vlg appked blw drain & source] and V_{GS} [Vlg appked blw gate & source.

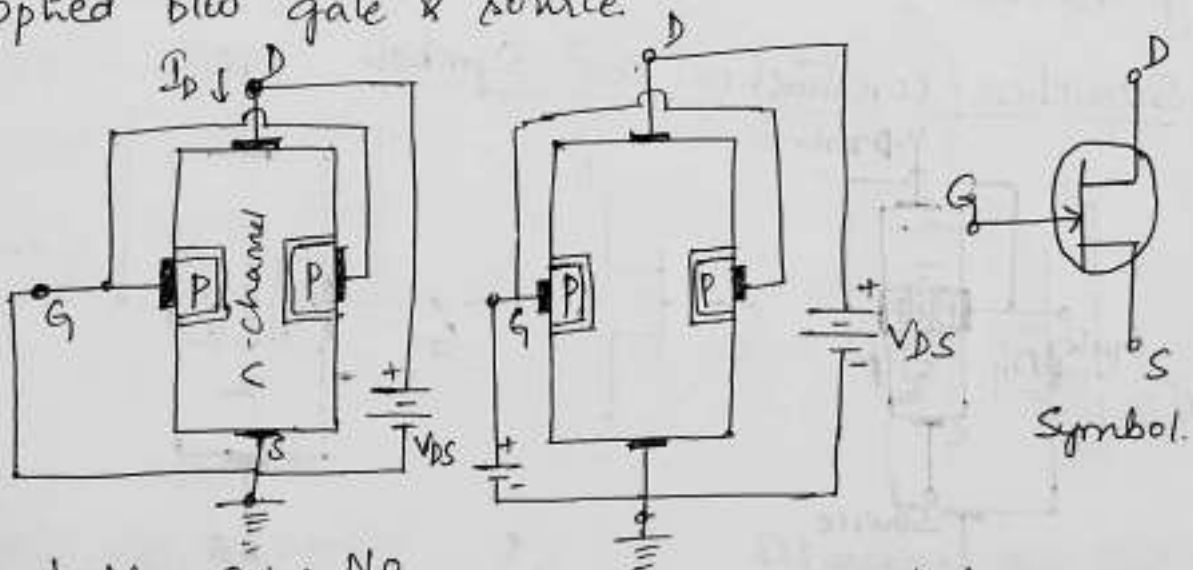


fig: a) $V_{GS}=0$ i.e No bias Vlg is appked at gate

b) V_{GS} = a small bias Vlg is appked at gate.

Case i) when $V_{GS}=0$ and V_{DS} = +ve potential.

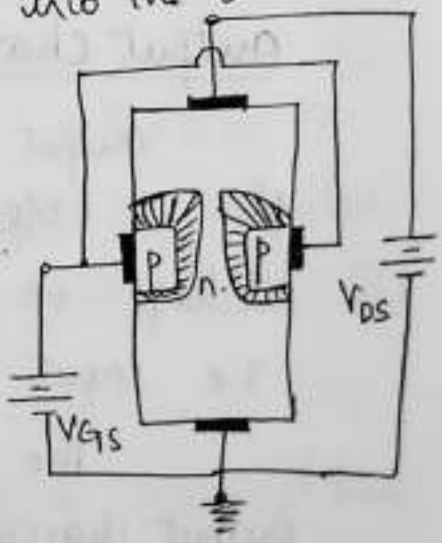
when positive Vlg is appked at the drain. & connecting gate terminal to ground i.e $V_{GS}=0$

i.e the p-n junction blw gate and source is constantly kept in reverse biased conditions. Since the p-n junction is reverse biased there will be very small amount of current or eventually it is zero. i.e $I_G = 0$. Because of the V_{DS} applied blw the drain & source, which attaracts the electrons from the n-material which leads to flow of current from Drain to source as shown in figure.

Case② when $V_{GS} < 0$ and $V_{DS} > 0$.

Due to connected vlg, the majority carriers i.e electrons begin to flow from source to drain reducing the depletion region and increases the channel width this stream of electrons makes the drain current. I_D.

Since gate is heavily doped and the channel is lightly doped, the width of the depletion region will spread in the channel. Since n-material is resistive, the drain current causes a vlg across the channel. This vlg drop reverse biases the p-n junction and causes the depletion regions to penetrate slowly into the channel.



when the large negative gate source vlg is applied the depletion region penetrates more into the n-channel. The depletion region width is more at drain side compared to source side as shown in figure. As we go on increasing negative vlg across gate source the depletion regions almost touch each other

which makes drain current to reduce.

Construction and Working of p-channel JFET

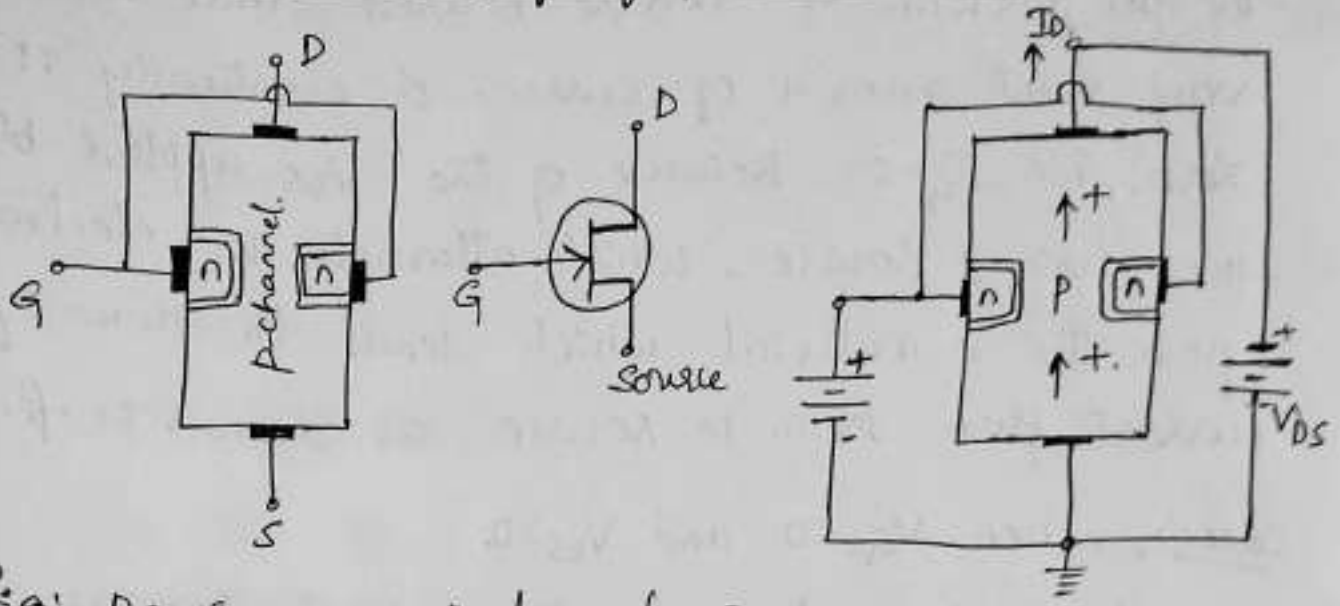


fig: Biasing of p-channel JFET.

The p-channel JFET is constructed similar to the n-channel JFET but with reversal of p and n-type material as shown in figure above. Here all the current and voltage applied will be reversed.

Channel width is maximum for $V_{GS}=0$. The channel width is reduced by increasing positive gate to source voltage V_{GS} is +ve for p-channel and V_{DS} is negative.

Output Characteristics / Drain Characteristics

Output & Drain characteristics of JFET is a plot of o/p current i.e Drain current versus output voltage i.e Drain to source v/g. Keeping V_{GS} constant i.e input v/g constant.

The experimental setup for measuring the output characteristics are as shown below.

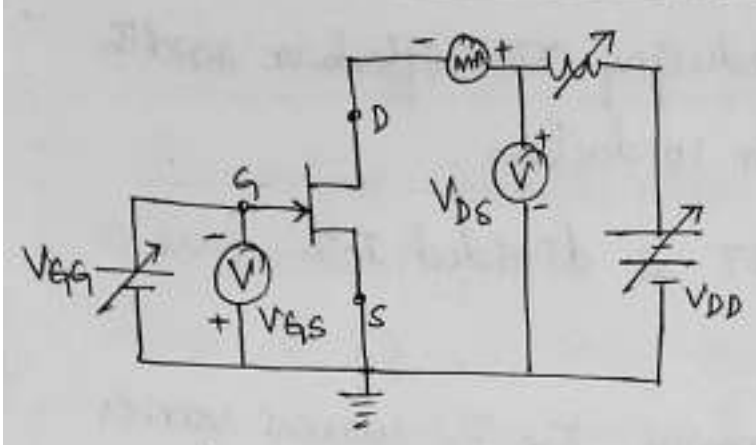
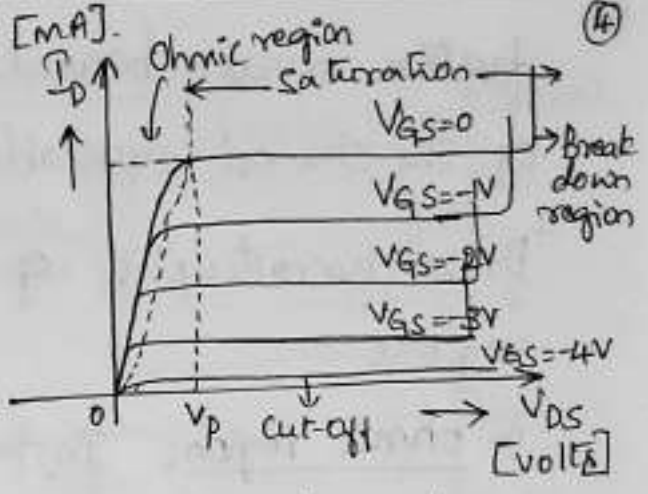


fig: Experimental setup to plot JFET characteristics



Drain characteristics.

1) when $V_{GS} = V_{DS} = 0$. The channel is entirely open. as $V_{DS} = 0$ there is no attarachive force for the majority carriers and hence drain current does not flow.

2) when $V_{GS} = 0$ and when a small amount of V_{DS} is applied. The drain current starts to flow. As we increase V_{DS} towards the +ve voltage. it increases the reverse bias on gate source junction and causes depletion region to penetrate into the channel reducing the channel width making the Drain current to be constant.

At some value of V_{DS}, the drain current I_D cannot be increased further due to reduction in channel width. The voltage at which I_D reaches to its constant saturation level is called "pinch off" voltage (V_p).

when the external bias of -V is applied blw the gate and source. the gate channels junctions

further reverse biased reducing the effective width of the channel available for conduction.

Drain characteristics of JFET is divided into four regions.

1) **ohmic region:** In this region, the I_D current varies linearly with V_{DS} satisfying the ohm's law hence the name ohmic region.

2) **Saturation region:** This is the region, in which I_D current remains constant and does not vary with V_{DS}.

3) **cutoff:** when V_{GS} made sufficiently negative, I_D is reduced to zero. This is caused by widening of depletion region to point where it completely closes the channel. V_{GS} at cut-off is called $V_{GS(off)}$

4) **Breakdown Region:** If V_{DS} is keep on increasing, the voltage will be reached at which gate channel junction breaks down due to avalanche effect. At this point the drain current increases very rapidly and device may be destroyed.

I_{DSS} is the maximum drain current when $V_{GS} = 0$. It is the saturated current blw the drain & source.

Drain characteristics of p-channel JFET:

The output characteristics of p-channel JFET is as shown in fig. In this the source is positive w.r.t to the drain. It is similar to the n-channel JFET except the voltages V_{GS} and V_{DS} have reversed polarities and current I_D flows in reverse direction.

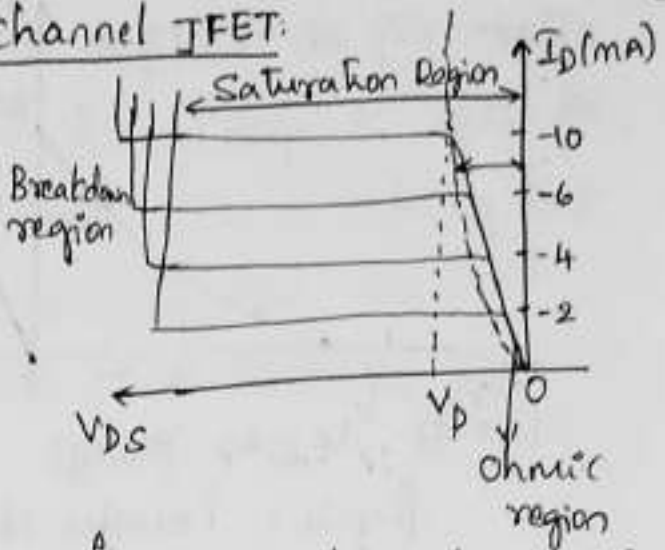


fig: Drain characteristics & VI characteristics of p-channel JFET.

Transfer characteristics of JFET

It is a plot of output current i.e I_D [Drain current] to input voltage i.e V_{GS} [Gate to source v/g] keeping V_{DS} constant.

The relationship blw I_D & V_{GS} is non-linear. This characteristic is defined by the equation

$$I_D = I_{DSS}\left[1 - \left(\frac{V_{GS}}{V_p}\right)\right]^2$$

where I_D → Drain current V_p → Constant
I_{DSS} → constant V_{GS} → control variable.

As V_{GS} decreases I_D increases exponentially. The transfer characteristics of JFET is drawn using,
i) Equation ii) o/p & Drain characteristics.

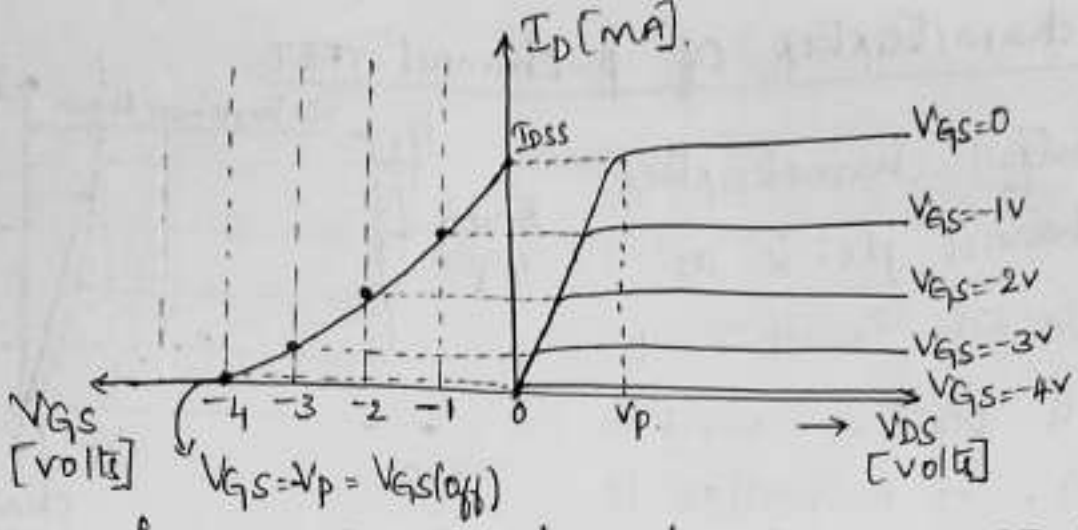


figure: Transfer characteristics of JFET using Drain characteristics.

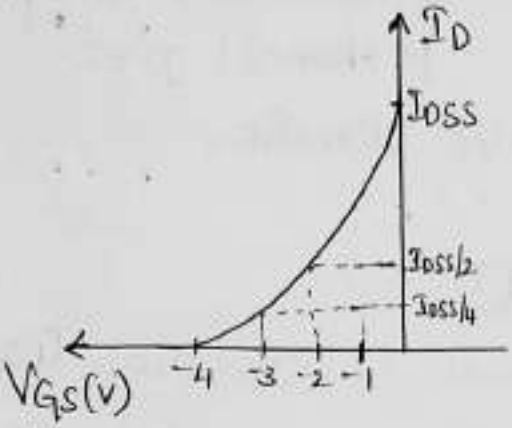


fig: Transfer characteristics of n-channel JFET

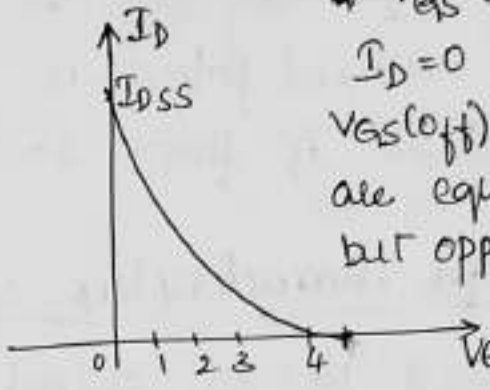


fig: Transfer characteristics of p-channel JFET.

* V_{GS} at which $I_D=0$ is called $V_{GS(off)}$. V_p & $V_{GS(off)}$ are equal in magnitude but opposite in sign.

The above figures shows the Transfer characteristic of n-channel JFET and p-channel JFET. p-channel JFET is similar to the n-channel JFET the only change is that the polarities of V_{GS} and I_D are reversed.

Characteristic parameters of JFET

1) Transconductance (g_m)
2) Input resistance
3) Drain to source resistance (r_d)
4) Amplification factor (μ)
5) power dissipation.

1) Transconductance: (g_m) : It is defined as the ratio of change in drain current for change in gate to source V_{GS} with V_{DS} = constant. It is nothing but the slope of the transfer characteristics of JFET. g_m is also called as mutual conductance. The unit is mS (millisiemen) or mA/V.

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS}=\text{constant}}$$

g_{mo}: It is transconductance measured at $V_{GS}=0$. It is normally given in the datasheet. The approximate value of g_m at any point on the transfer characteristics is calculated using.

$$g_m = g_{mo}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]$$

When g_{mo} is not given in the data sheet:

$$g_{mo} = \frac{2 I_{DSS}}{|V_{GS(off)}|}$$

2) Input Resistance: JFET operates with its gate-source junction reverse biased, which makes the input resistance at the gate very high. The input resistance can be determined by. $R_{IN} = \left|\frac{V_{GS}}{I_{GSS}}\right|$

I_{GSS} will be given in datasheet. I_{GSS} is gate reverse current. The gate reverse current increases with temperature

thus decreases the i/p resistance.

3) AC drain to Source resistance (r_d)

The drain resistance r_d is the ac resistance b/w drain and source terminals when JFET is operating in saturation region. r_d is given by,

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS} = \text{constant}}$$

Above pinch off, the drain current is relatively constant over a range of drain to source v/g. Large change in V_{DS} produces very small change in I_D. Since characteristic is flat in saturation region, r_d is not easily determined. It may also be expressed as an output admittance. The admittance is given by the expression.

$$Y_{os} = \frac{1}{r_d}$$

4) Amplification factor: (μ)

The amplification factor is defined as rate of change of drain to source v/g to rate of change of gate to source v/g keeping drain current constant. The expression for amplification factor is given by,

$$\mu = \left.\frac{\Delta V_{DS}}{\Delta V_{GS}}\right|_{I_D \text{ is constant.}}$$

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \cdot \frac{\Delta I_D}{\Delta V_{GS}} = r_d \cdot g_m.$$

5) Power Dissipation: (P_D)

Power dissipation can be defined as product of drain current and drain to source vlg. The expression for power dissipation can be given by.

$$P_D = I_D \cdot V_{DS}$$

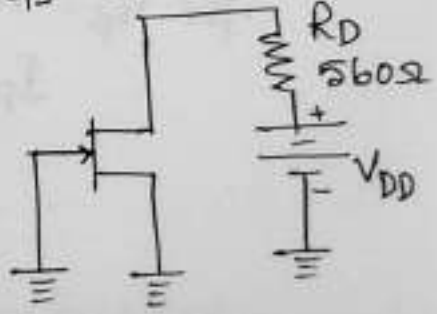
JFET Transfer characteristic is expressed by.

$$I_D \cong I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

The above equation is also called as 'Square Law' & Drain current equation for JFET. I_D can be determined for any V_{GS}, if $V_{GS(off)}$ and I_{DSS} is known. I_D is function of square of appled i/p voltage V_{GS} Hence the name "Square law"

problems:

1) For the JFET shown in fig: $V_{GS(off)} = -4V$ and $I_{DSS} = 12mA$. Determine the minimum value of V_{DD} required to put the device in the constant current region of operation when $V_{GS} = 0V$



Soln: Given $R_D = 560\Omega$, $V_{GS(off)} = -4V$

$\therefore V_p = 4V$, $I_{DSS} = 12mA$.

The minimum value of V_{DS} for the JFET to be in Constant current region is $\boxed{V_{DS} = V_p = 4V}$

In the constant-current region with $V_{GS} = 0V$

$$I_D = I_{DSS} = 12mA.$$

The drop across R_D is

$$V_{RD} = I_D \times R_D = (12mA)(560\Omega)$$

$$\boxed{V_{RD} = 6.72V}$$

Applying Kirchhoff's law around the drain ckt

$$V_{RD} = V_{DS} + V_{RD}$$

$$= 4 + 6.72$$

$$\boxed{V_{DD} = 10.72V}$$

This is the V_{DS} at V_{DD} to make $V_{DS} = V_p$ and put the device in the constant current region.

2) For a 2N5459 JFET, it is given $I_{DSS} = 9mA$ and $V_{GS(off)} = -8V$ (maximum). Using these values determine the drain current for $V_{GS} = 0V$, $-1V$ and $-4V$.

Sol^n: $V_{GS} = 0V$,

$$I_D = I_{DSS} = 9mA.$$

for $V_{GS} = -1V$,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

$$= (9mA)\left(1 - \frac{-1V}{-8V}\right)^2$$

$$= 9 \times 10^{-3}(1 - 0.125)^2$$

$$\boxed{I_D = 6.89mA}$$

for $V_{GS} = -4V$

$$I_D = (9mA)\left(1 - \frac{-4V}{-8V}\right)^2$$

$$= 9\times10^{-3}(1-0.5)^2 = 9\times10^{-3}\times0.25$$

$$\boxed{I_D = 2.25\,mA}$$

3) The following information is included in the datasheet of 2N5457 JFET. typically, $I_{DSS} = 3.0mA$, $V_{GS(off)} = -6V$ maximum and $g_{mo} = 5000\mu s$. Using these values determine the forward transconductance for $V_{GS} = -4V$ and I_D at this point.

Soln: $g_{mo} = 5000\mu S$, $I_{DSS} = 3\times10^{-3}A$, $V_{GS(off)} = -6V$

$$g_m = g_{mo}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]$$

$$= 5000\left(1 - \frac{-4V}{-6V}\right]$$

$$\boxed{g_m = 1667\mu S}$$

$$I_D \cong I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

$$= 3\times10^{-3}\left[1 - \frac{-4}{-6}\right]^2$$

$$\boxed{I_D = 333\mu A}$$

4) A Given JFET has following characteristics: $I_{DSS} = 12mA$, $V_{GS(off)} = -5V$ and $g_{mo} = 3000\mu S$ Find

g_m and I_D when $V_{GS} = -2V$.

Soln: Given: $I_{DSS} = 12mA$, $V_{GS(off)} = -5V$ and $g_{m0} = 3000\mu S$

$V_{GS} = -2V$.

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]$$

$$= 3000 \times 10^{-6}\left[1 - \frac{-2V}{-5V}\right]$$

$$\boxed{g_m = 1800\mu S}$$

$$I_D \cong I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

$$= 12 \times 10^{-3}\left[1 - \frac{-2}{-5}\right]^2$$

$$\boxed{I_D = 4320\mu A}$$

A) A Certain JFET has an I_{GSS} of $-2nA$ for $V_{GS} = -20V$. Determine the input resistance

Soln: given: $I_{GSS} = -2nA$

$V_{GS} = -20V$

$$R_{IN} = \left|\frac{V_{GS}}{I_{GSS}}\right|$$

$$= \frac{20V}{2nA}$$

$$\boxed{R_{IN} = 10,000 M\Omega}$$

METAL OXIDE SEMICONDUCTOR FET [MOSFET]

This is very small hence can be used to design high density VLSI ckts. MOSFETs has no pn junction structure. Instead the gate of MOSFET is insulated from channel by a SiO_2 layer. Due to this i/p resistance is very high.

Because of the insulated gate, they are also called as IGFET's [Insulated Gate FET's].

They are two types.

1) Depletion (D) MOSFET
2) Enhancement (E) MOSFET.

Enhancement MOSFET (E-MOSFET)

E-MOSFET operates only in the enhancement mode and has no depletion mode. There is channel exist blw Drain and the source. We have to create & enhance a channel blw drain and the source hence the name Enhancement MOSFET.

Below figure shows the structure of E-MOSFET.

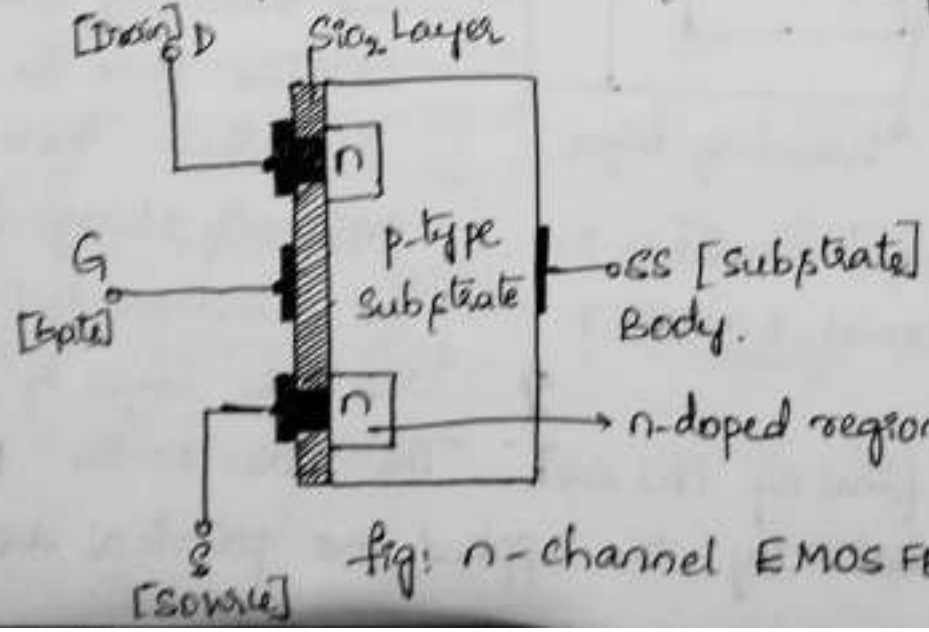


fig: n-channel EMOSFET.

Construction: Two highly doped n regions are diffused into a lightly doped p-type substrate. The source and drain are taken out through metallic contacts to n-doped regions as shown in fig.

There is no direct contact of the gate terminal with the substrate. There is a layer of SiO_2 which acts as a barrier & insulator blw gate terminal and the substrate. It has four terminals. Gate, Drain and the source along with substrate (SS) terminal & body. The substrate and the source terminal is always interconnected. There is no channel exist blw Drain and the source under no bias condition.

Operation:

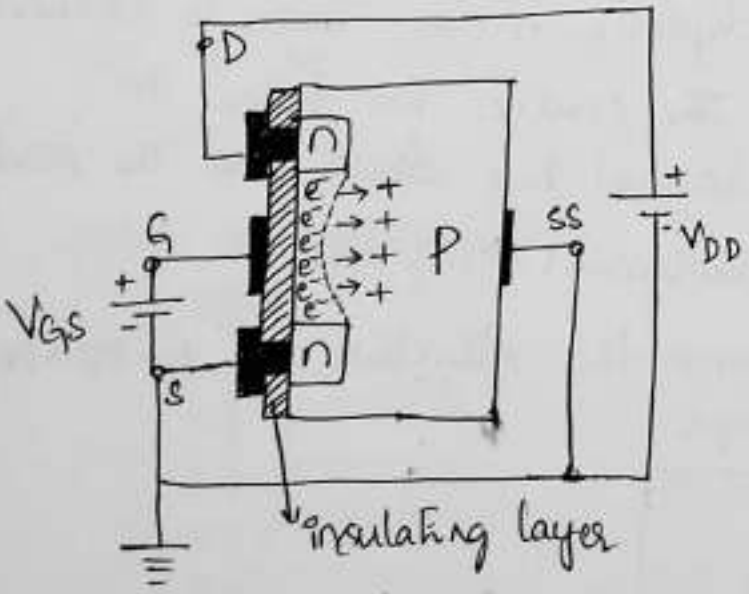


fig: Channel formation in n-channel E-MOSFET

When a +ve vlg V_{GS} is applied blw the gate and the source terminal as shown in fig.

The +ve potential at the gate terminal attracts the minority charge carriers from the p-type substrate. These attracted minority charge carriers i.e electrons get accumulated over the layer of p substrate thereby forming channel. The holes in the p substrate gets repelled by the applied +ve potential and will be

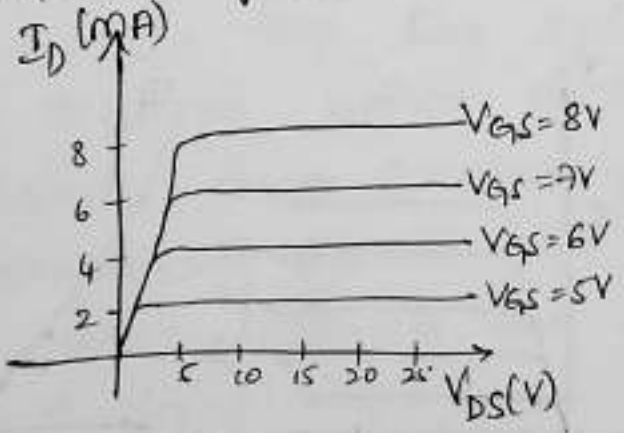
pushed down. The attaracted elections will not be able to cross the gate terminal because of the layer of SiO_2 which acts as barrier and prevents the electrons in the induced channel from being attaracted by gate terminal

The Vlg applied blw Drain and the source i.e V_{DS} attaracts the elections which will cause the flow of I_D current through the induced channel. As V_{GS} increased more elections will be attaracted and hence increases the I_D current.

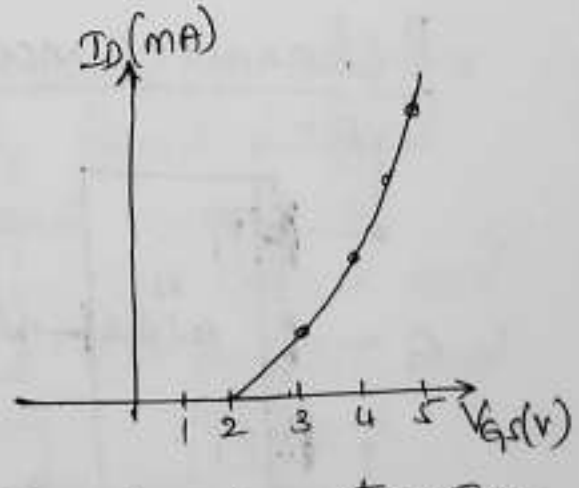
The lowest value of V_{GS} for which these exist I_D current just starts flowing is called "Threshold voltage" (V_T).

Channel does not exist with $V_{GS} = 0V$ and enhanced due to application of a +ve gate to source Vlg. Hence the name enhancement MOSFET.

The Drain characteristics and Transfer characteristics are given below.



Drain characteristics



Transfer characteristics.

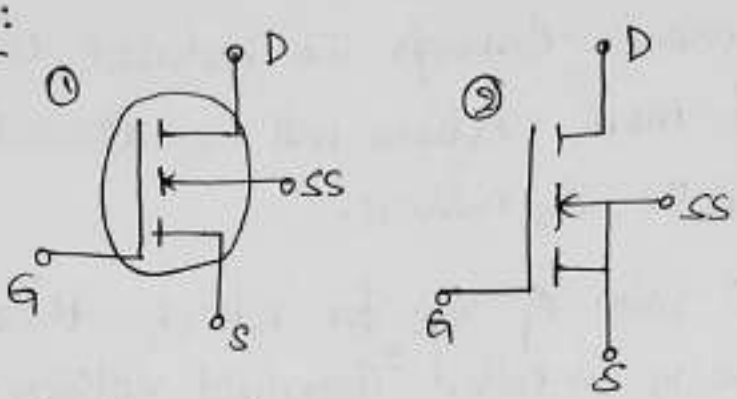
For n-channel MOSFET V_{GS} is +ve and I_D does not flow until $V_{GS} = V_T$.

For $V_{GS} > V_T$ the relationship b/w drain current and V_{GS} is non-linear and it is given by

$$\boxed{I_D = K(V_{GS} - V_T)^2}$$

K = Constant $\qquad K = \dfrac{I_{D(ON)}}{(V_{GS(ON)} - V_T)^2}$

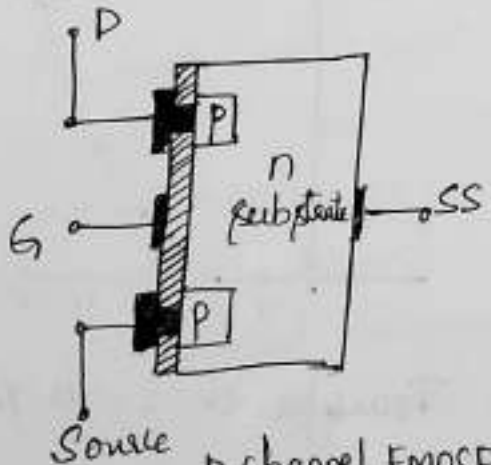
Symbol:



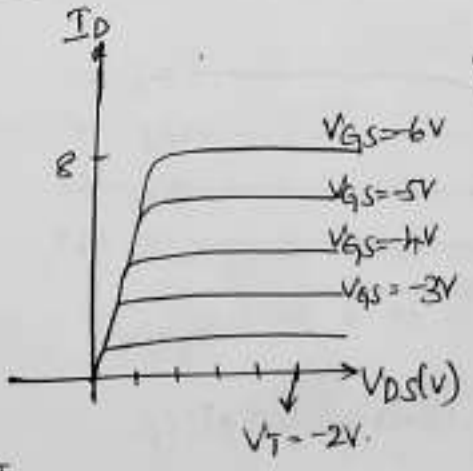
n-Channel E-MOSFET.

The dotted line indicates that there is no channel b/w Drain and the source. In some cases substrate and the sources will be interconnected which is shown in fig②

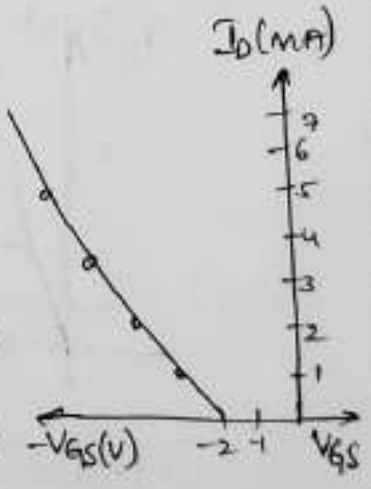
P-Channel E-MOSFET:



p-channel EMOSFET Structure

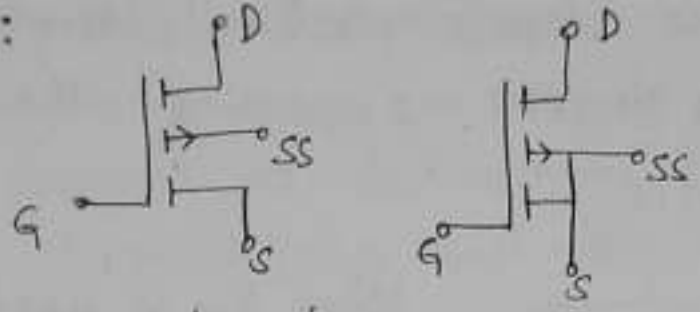


Drain Characteristics



Transfer Characteristics

Symbol:



p-channel E-MOSFET.

p channel E-MOSFET is exactly opposite to that of n-channel MOSFET. Construction, Drain characteristics, Transfer characteristics and Symbol are as shown in above fig.

Note: p-channel E-MOSFET and D-MOSFET construction and operation you need to study by yourself.

Depletion MOSFET (D-MOSFET)

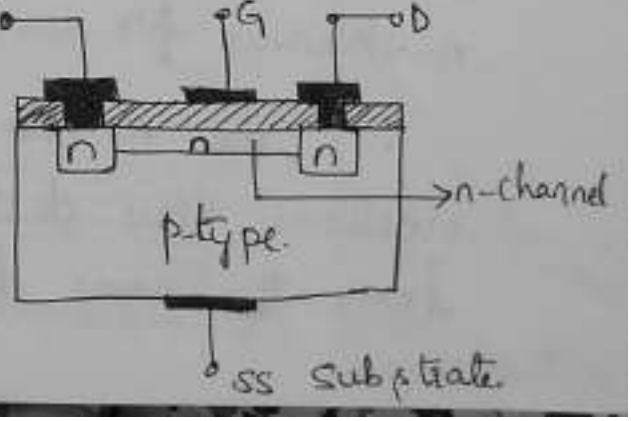
In this type of MOSFET, there exist a depletion layer or channel blw the drain and the source under no bias condition.

n-Channel D-MOSFET:

In this two specially doped n-regions are diffused within a lightly doped p-typed substrate. These enormously doped n-regions characterises source and drain. The source and the drain terminals are linked via metallic bond to n-doped regions.

attached via n-channel.

The gate is also connected to metal surface but insulated by a very thin layer of SiO_2.



Thus there is no direct electrical connection blw gate & channel of a MOSFET, increasing the input impedance of device.

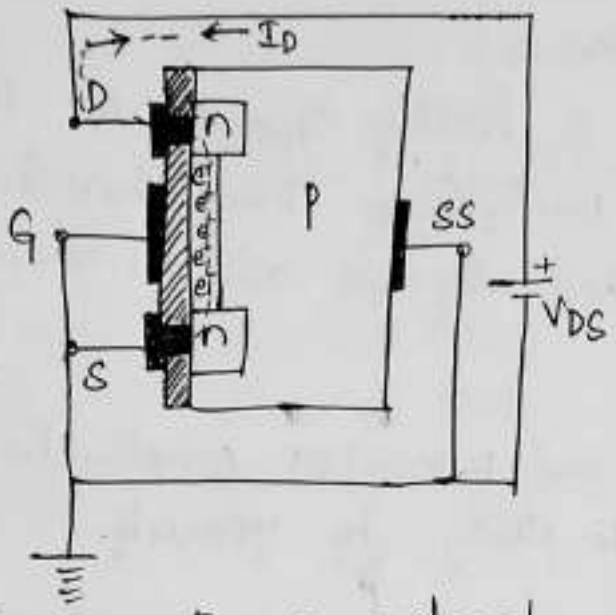


fig: Operation of n-channel D-MOSFET

When V_{DS} is applied keeping $V_{GS}=0$ by directly connecting gate to source terminal free electrons from the n-channel are attracted towards +ve potential of drain terminal.

This establishes current through the channel to be denoted as I_{DSS} at $V_{GS}=0V$.

If we apply -ve voltage across the gate and source terminal. the negative charges on the gate terminal repel and get attracted by the +ve charges in the substrate. This initiates a recombination of repelled electrons and holes from the p substrate. This recombination depends on magnitude of negative voltage applied to the gate. Hence the number of free electrons reduced due to the recombination in n-channel for conduction reducing the Drain current.

The n-channel is depleted some of its electrons thus decreasing the channel conductivity hence the name depletion MOSFET.

The greater the depletion of n-channel electrons with increasing negative bias for V_{GS}. the level of drain current will deduced as shown. In fig. The Drain characteristics and the Transfer characteristics are as shown below.

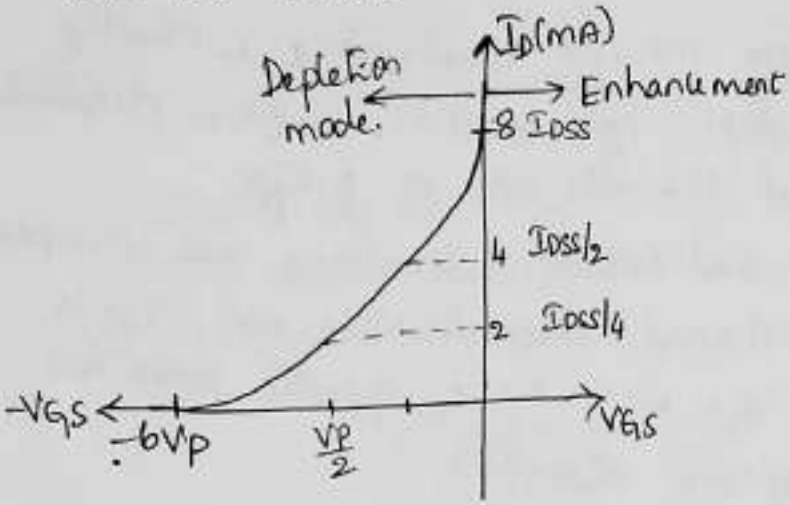


fig: Transfer characteristics

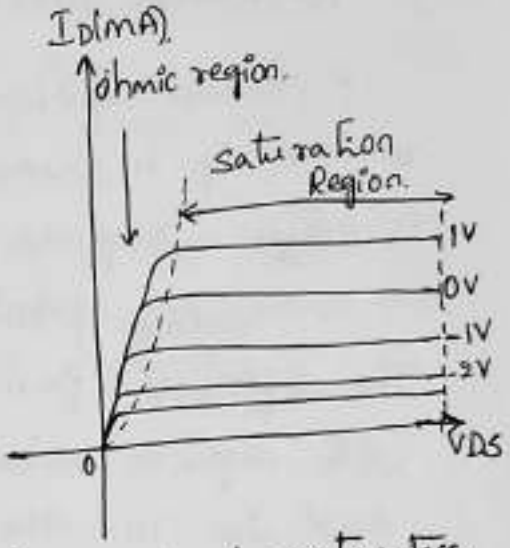
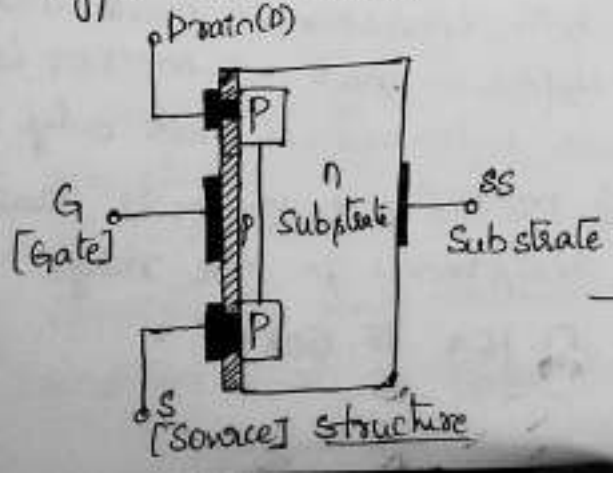


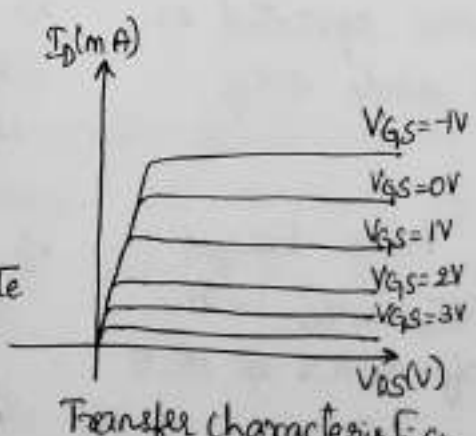
fig: Drain characteristics

If the positive voltage is applied b/w the gate and source terminal. which enhances the number of electrons in the channel in contrast to that observed with $V_{GS}=0$. Hence the region of positive gate voltage on the transfer characteristics can be referred as enhancement region.

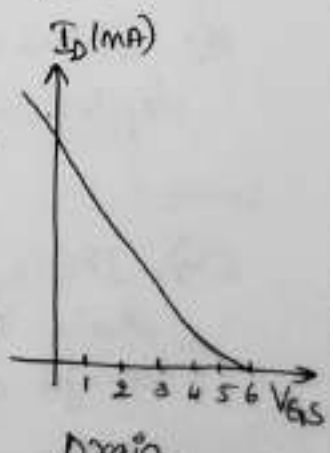
p-channel Depletion Type D-MOSFET

The below figures shows the structure. transfer characteristics and Drain characteristics of p-channel type D-MOSFET.



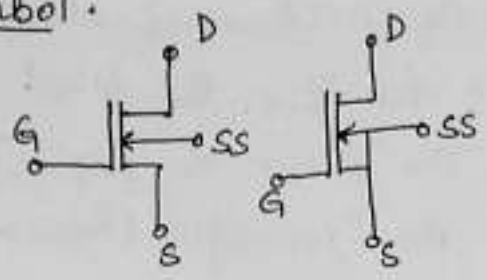


Transfer characteristics

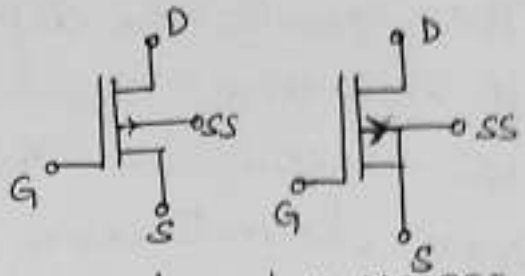


Drain characteristics

Symbol:



n-channel DMOSFET.



p-channel D-MOSFET.

P-channel depletion type MOSFET construction is exactly reverse of n-channel depletion type MOSFET. In this substrate is n-type, regions and channels are of p-type

Voltage polarities and current directions are reversed. The difference from n-channel characteristics are, V_{DS} is with negative values. V_{GS} will have opposite polarities. and I_D in the opposite direction.

Comparision between JFET & MOSFET

JFET's	MOSFET's
1) JFET is fabricated using a semiconductor bar which acts as a channel	1) MOSFET is fabricated on a semiconductor substrate
2) Fabrication process is complex.	2) Fabrication process is simple and easy
3) JFET does not contain an insulating silicon dioxide layer	3) MOSFETs are fabricated with SiO_2 Layer.
4) JFETs are operated in depletion mode only	4) D-MOSFET is operated in both enhancement mode and depletion mode. E-MOSFET is in Enhancement mode only.
5) JFETs have larger drain resistance in the range of 100kΩ to 1MΩ	5) MOSFETs have lower drain resistances in the range of 1kΩ to 50kΩ.

6) The input resistance offered by JFET are lesser in the range of 1GΩ to 10GΩ	6) The input resistance offered by MOSFET are much higher in the range of $10^{13}\Omega$ to $10^{15}\Omega$
7) The leakage current is more in JFETs in the range of 10nA to 100μA	7) The leakage current is much lesser in MOSFETs in the range of 1pA to 100pA.
8) JFETs are not so widely used in electronic and computer Industries	8) MOSFETs are extensively in digital electronics and computer industry.

CMOS

Complementary metal oxide semiconductor [CMOS] technology is one of the most popular technology in the computer chip design industry and broadly used for integrated circuits in numerous and varied applications.

All the computer memories, CPUs and cell phone make use of this technology. for microprocessors, microcontroller chips, and also memories like RAM, ROM, EEPROM and application specific integrated circuits [ASICs]

CMOS transistor consists of both P-channel MOS [PMOS] and N-Chanel MOS [NMOS].

CMOS Inverter

CMOS inverter is a transistor made up of two complementary transistors. It consists of n-channel & p-channel on a single substrate. The CMOS inverter consists of two transistor types which are processed and connected as shown in fig.

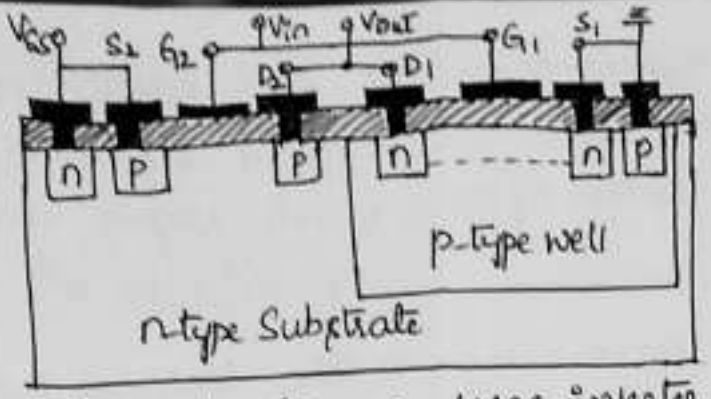


fig: structure of CMOS inverter.

The Inverter is a logic ckt which is going to invert the given input. i-e complement of the input will be obtained as output. If the inputs are high o/p will be low. And if the I/p is low o/p will be high.

The complementary N-type and p-type E-MOSFETs are connected in series. The gate terminals are connected together to form input terminal. The output terminal is formed by connecting drain terminals together. Source terminal S_1 is connected to ground and source terminal S_2 is connected to voltage V_{SS}.

The simplified diagram of CMOS inverter using two transistor and as switch is as shown in fig below.

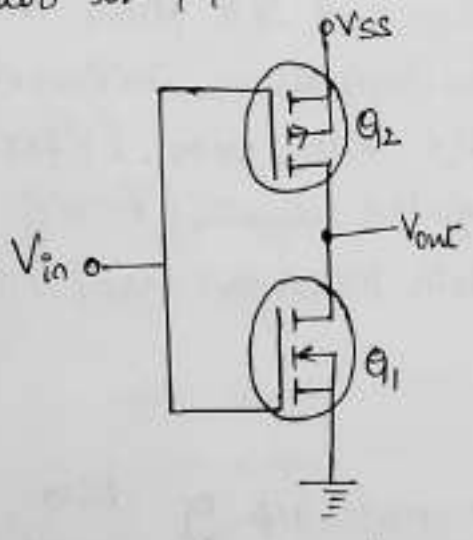


fig: Simplified diagram of CMOS inverter

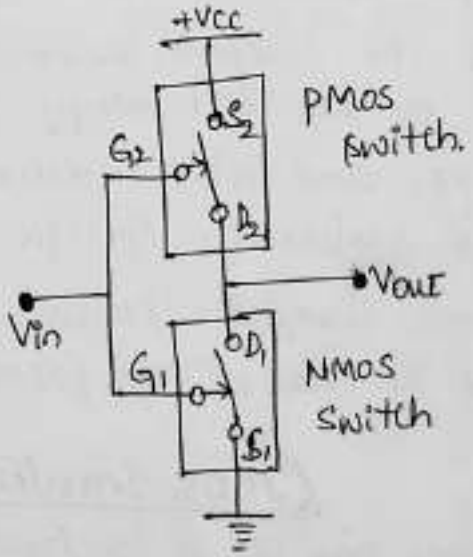


fig: CMOS inverter operation using switch.

Case i: When V_{in} is Low, the gate source voltage ($V_{G_2S_2}$) of p channel is equal to $-V_{SS}$. The PMOS will get activated

i.e PMOS switch will be closed providing low resistance path blw V_{SS} and o/p terminal. Since gate source vlg $V_{G_1S_1}$ of N-channel EMOSFET is 0V. It will be in the OFF state. which results in high impedance blw the output & ground. Hence V_{out} is equal to supply vlg V_{SS} i.e V_{out} = High.

Case ii) when V_{in} = High.

the gate source vlg ($V_{G_2S_2}$) of the PMOS is equal to 0V. The PMOS will be in OFF state providing high resistance. The gate source vlg ($V_{G_1S_1}$) of the NMOS is equal to V_{SS}. which will turn ON NMOS. which provides less impedance and o/p terminal will be connected with Ground. which gives V_{out} = Low.

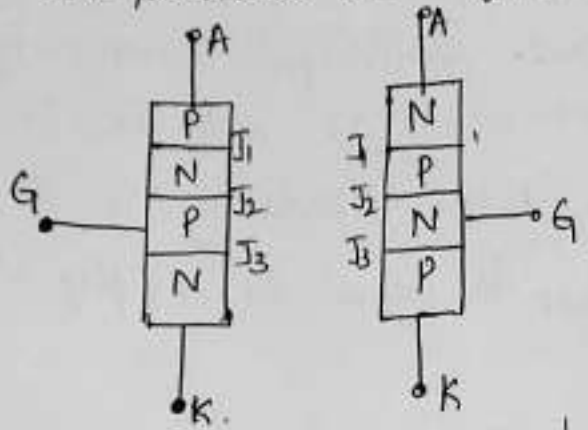
This CMOS inverter has low power dissipation because only one MOSFET will be in ON state at a time.

Silicon Controlled Rectifier [SCR]

A Silicon Controlled Rectifier (SCR) is a four-layer unidirectional semiconductor device made of silicon which can be used to provide a selected power to the load by controlling the current. SCRs are also called as Thyristor. [SCR is a one type of Thyristor].

SCR is a three terminal device with four layers. hence it has three junctions J_1, J_2, J_3. The four layers are alternate p and n type material. It is nothing but a rectifier and junction transistor. The two types are, NPNP and PNPN SCRs. The three terminals are, Anode (A), Cathode (K) and Gate [G]

The structure and Symbol is as shown in fig below.



PNPN structure

NPNP structure.

Symbol.

To forward Bias the SCR, connect Anode to +ve of supply vlg. which makes J_1 & J_3 forward bias and J_2 reverse bias w.r.t applied vlg.

To Reverse Bias the SCR connect Anode to -ve of supply vlg. which makes J_1 & J_3 Reverse bias and J_3 forward bias w.r.t applied vlg.

In PNPN SCR, the outer most player is taken as Anode terminal. the outer most N-layer is taken as cathode terminal. The gate terminal is taken out from the player which is near to cathode terminal.

SCR can be operated in three different modes

1) Forward blocking mode
2) Forward Conduction mode
3) Reverse blocking mode.

Working of SCR:

The anode terminal is connected to positive terminal of power supply, cathode terminal is connected to negative terminal of power supply and positive pulse vlg are applied at gate terminal. The SCR is forward biased.

The current starts flowing from anode to cathode This mode is called forward conduction mode. Once it is forward biased there is no need to apply any voltages at gate terminal. Gate terminal is used to just to Trigger the circuit.

SCR would be in ON State until it would turned OFF. The SCR can be turned off by reducing gate vlg & by shorting Anode & cathode together through transistor & push button.

Two Transistor Model

If we take the cross sectional of SCR. we can see two transistors connected back to back as shown in figure below. The two transistors are NPN & PNP transistors.

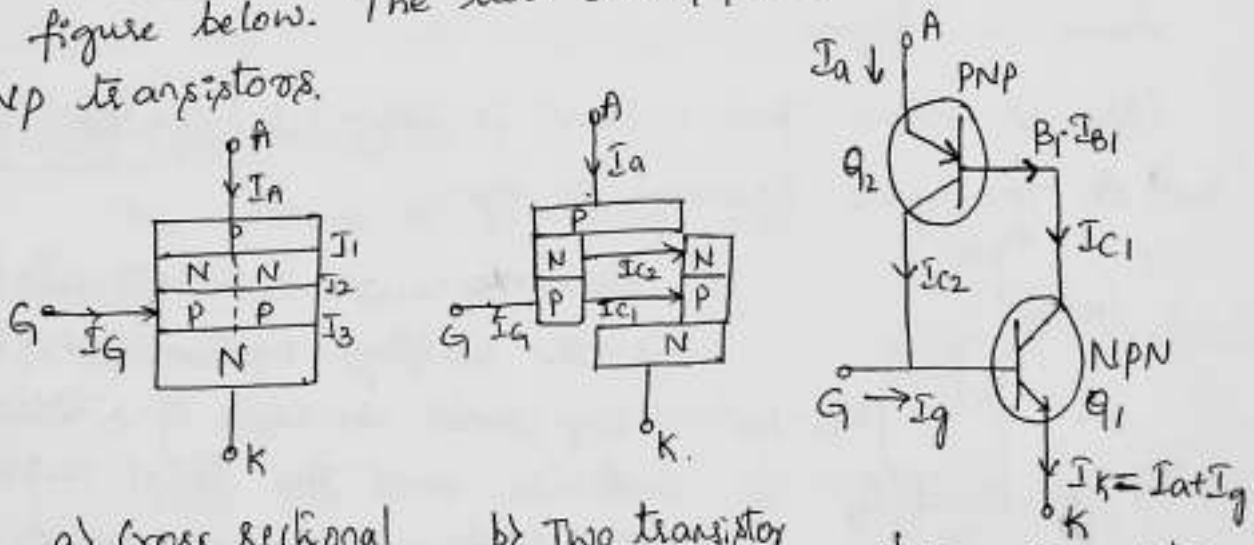


fig: a) Cross sectional view b) Two transistor model c) Two transistor equivalent model.

The upper left one is PNP transistor and the lower right NPN type. The two transistors are connected in such way that the collector of NPN is connected base of the PNP and the collector of PNP is connected to base of NPN transistor And the gate terminal is brought out from the base of NPN.

∴ The o/p of one transistor will act as an input to other transistor i.e.

for Q_1 transistor:

$$I_{C_1} = \beta_1 \cdot I_{B_1} \qquad I_{C_2} = \beta_2 \cdot I_{B_2}$$

$$I_{B_2} = I_{C_1}$$

$$\therefore I_{C_2} = \beta_1 \cdot I_{B_1} \cdot \beta_2$$

$$I_{C_2} = \beta_1 \cdot \beta_2 \, I_{B_2}.$$

This gives net gain of loop ckt as $\beta_1 \times \beta_2$ where β_1 & β_2 are current gains of two transistors.

Switching Action

Let us consider two transistor model of SCR as shown in figure.

Case i) when gate current is zero i.e $[V_G = V_{BE} = 0]$ & the gate terminal is open.

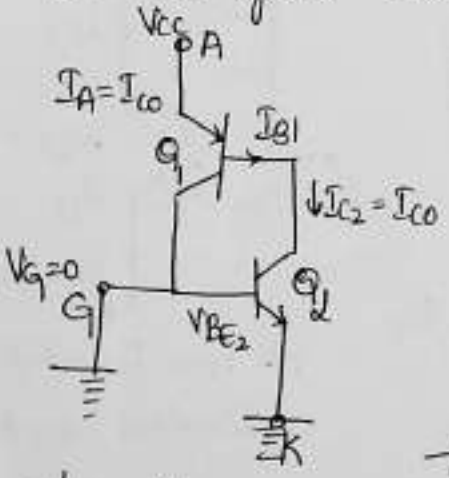


fig: When $V_G = 0$.

The only current in circulation is the leakage current which is very small in case of silicon device and the total current is little higher than the sum of individual leakage current. Under this condition SCR is said to be in forward blocking mode & High impedance state & OFF state.

Case ii) V_G = a small vlg.

When small amount of gate current is given to the base of transistor Q_2 i.e $V_{BE} = V_G$ by applying forward bias to its Base emitter junction as shown in fig.

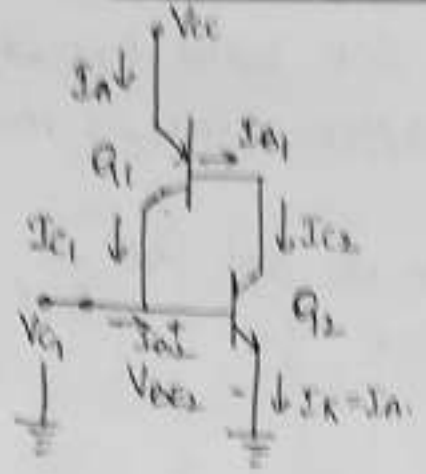


fig: With Vg applied

The Vg applied generates base current to Q_2 i.e I_{B_2} which in turn gives I_{C_2} which is β_2 times the I_{B_2}.

The collector current of Q_2 is fed as i/p current of Q_1 and undergoes further amplification by multiplying I_{C_2} with β_1.

This way both the transistors feedback each other and the collector current of each goes on multiplying. This process is very quick and soon both drive each other to saturation. Now the SCR is in ON state. The SCR can be turned off & can control the current only through external ckt.

TURN OFF Methods.

The process of turning off a SCR is called Commutation. By the process of commutation the SCR operating mode is changed from forward conduction mode to forward blocking mode.

There are two methods of commutation of SCR

1) Natural commutation
2) Forced commutation.

Natural Commutation: The process of turning off a thyristor without using any external circuit is known as Natural commutation.

This type of commutation is possible only in AC applications. When using AC supply, the current passing through the device is alternating. This alternating current go to peak, zero and then through

peak negative value. Due to this SCR turns off when negative vlg appears across the SCR.

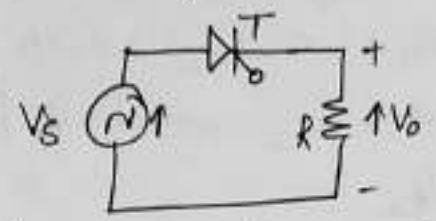


fig: Natural commutation

As there is no spl ckt to turn off SCR This is called Natural commutation.

2) **Forced commutation**: The process of turning off a SCR by using external circuits is called forced commutation. This method of commutation is used for DC commutation.

Since DC is unidirectional it can't make SCR to turn off. so external ckt to be connected to make current to be equal to zero forcibly. Hence it is called forced commutation and is also called DC commutation.

The external ckt used for commutation process is called as commutation ckt. and the elements are called as commutating elements.

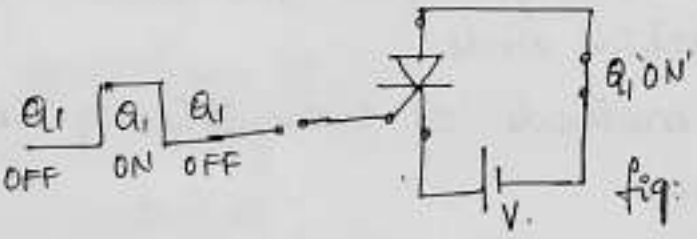


fig: Forced commutation.

Characteristics of SCR [V-I Characteristics]

The V-I characteristics of SCR is the plot of applied forward vlg versus Anode current I_A. The characteristics are as shown in figure.

The characteristics are divided into different region which are explained below. The characteristics are obtained by applying forward biasing.

1) Forward Breakover voltage: $V_{F(BO)}$
It is the vlg above which the SCR enters the conduction region. This vlg decreases as I_G increases.

2) Holding current: I_H is the value of current below which SCR switches from conduction state to forward blocking region under stated conditions

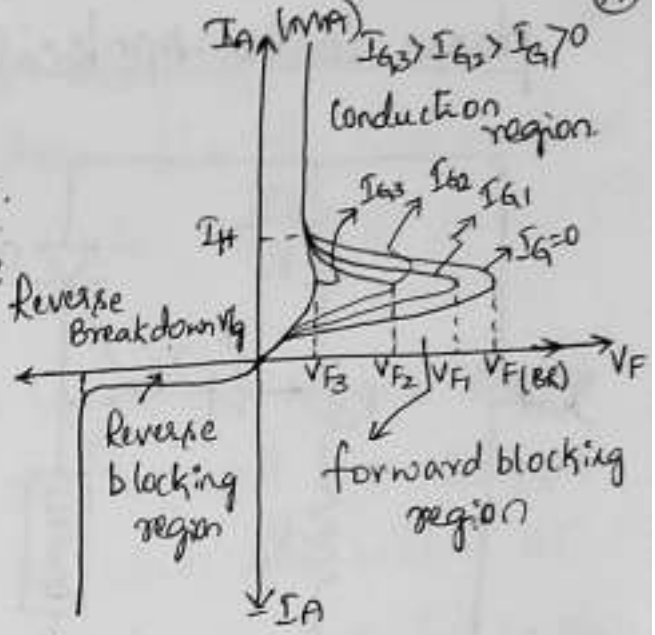


fig: V-I characteristics of SCR.

3) Forward & Reverse blocking Regions: These are the regions corresponding to the open ckt conditions for the SCR which blocks the flow of current from anode to cathode.

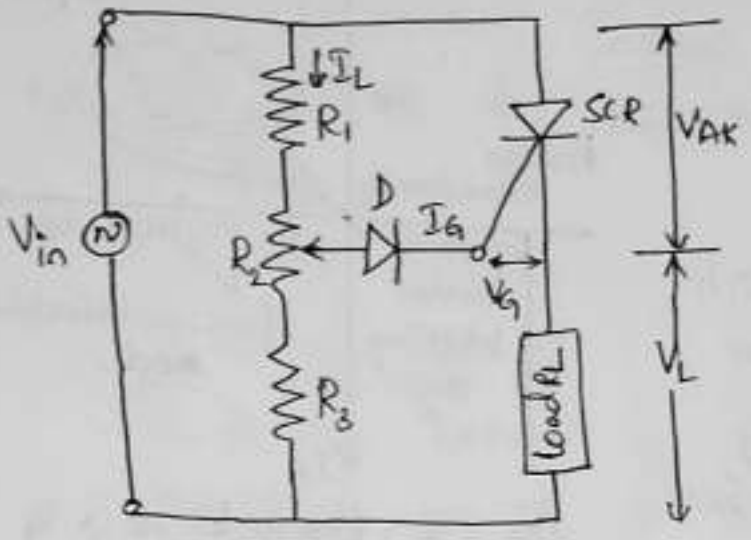
4) Reverse Breakdown vlg: It is the reverse anode to cathode vlg at which zener & avalanche breakdown takes place as in fundamental PN junction diode and raises the current abruptly.

Applications of SCR

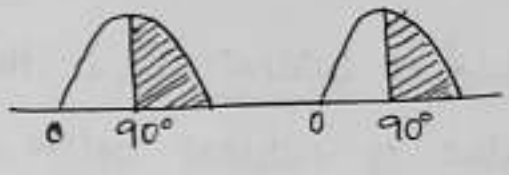
1) Switching 2) Rectification 3) Regulation
4) protection
5) Home appliances: Lighting, temperature control, fan speed regulation, heating and alarm activation
6) In industry: for motor speed, battery charging power conversions.
7) phase control.

One of the applications of SCR i.e phase control is discussed in detail.

phase control Application



phase control circuit



Firing angle.

* In ac ckt the SCR can be turned on by the gate at any angle α w.r.t to the applied vlg. This angle α is called the firing angle.
* Power control is obtained by varying the firing angle and is known as phase control.
* phase control ckt is as shown in fig above. The gate triggering vlg is derived from the ac supply through resistors R_1, R_2 and R_3. The variable resistance R_2 limits the gate current during positive half cycles of the supply. R_2 is a variable resistance.
* If the moving contact is set to top of resistor R_2, resistance R_2 will be very low and SCR may trigger almost immediately at the The commencement of the +ve half cycle.
* If the moving contact is set to bottom of the resistor R_2, resistance R_2 will have maximum, the SCR may not switch on until the peak of the +ve half cycle.

* By adjusting R_2 blw these two extremes, SCR can be switched on somewhere blw the commencement and peak of the +ve half cycle that is blw 0° & 90°
* If the triggering voltage V_T is not large enough to trigger SCR at 90°, the device will not trigger on at all, because V_T has the maximum value at the peak of the i/p and decreases with fall in vlg.
* This operation is also referred as half-wave variable resistance phase control.
* It is an effective method of controlling the load power
* Diode 'D' is provided to protect the 'SCR' gate from the negative vlg that would otherwise be appled during the negative half cycle of the input.

---x x---

module - 3

Operational Amplifiers And Applications

* The Operational Amplifier abbreviated as Op-Amp is the best known example of a general purpose Linear integrated circuit.

* Op-Amp is a directly coupled multistage voltage amplifier with high gain. It has very high input impedance and very low output impedance

* The Significance of 'operational' is that the Op-Amp can perform mathematical operations such as summation, subtraction. Differentiation, Integration. These operations are important in analog computers.

* Op-Amp can also be used in Signal amplification, wave forming, Servocontrols impedance transformation, Active filters, oscillators, voltage regulators, Analog to digital and Digital to analog converters.

Op-Amps are useful in communication equipment, instrumentation and data processing.

Circuit Symbol

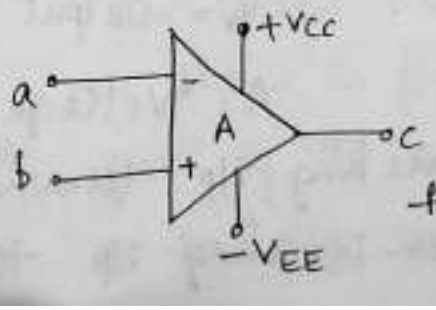


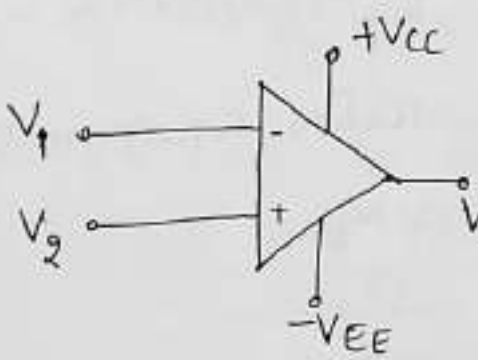
fig: Ckt Symbol of Op-Amp

It has two input terminals marked as a & b. The terminal 'a' is called 'inverting input' terminal. And is labelled with '−' sign. The terminal is 'b' is known as 'Non-inverting input' terminal. and is labelled with '+' sign. It has one output terminal labelled as 'c' in the above figure.

Since the op-Amp is an Active device, it requires a dc power supply for its operation. The power supply Vlgs which are usually balanced with respect to ground are applied to the terminals through $+V_{CC}$ & $-V_{EE}$.

The Op-Amp is also known as Differential Amplifier i.e The output vlg at terminal 'c' is proportional to the Difference of the two signal voltages applied at the two input terminals

i.e $\boxed{V_0 = A(V_2 - V_1)}$



A is a constant of proportionality called voltage gain of the op-Amp.

V_0 = Output voltage

A = Voltage gain of the op-Amp.

V_1 = Inverting i/p terminal voltage.

V_2 = Non-inverting i/p terminal voltage.

The most commonly used Op-Amp IC is IC741. pin diagram of IC-741 is.

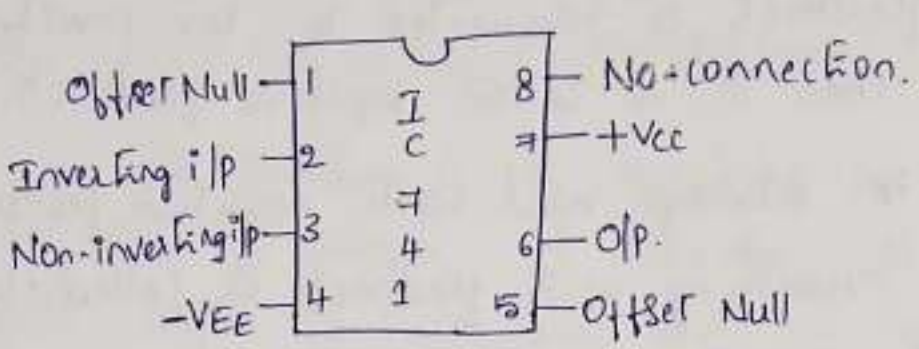
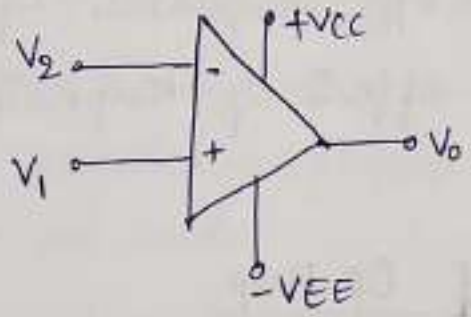


fig: pin-configuration of IC-741.

Op-Amp can be operated in two configurations.

1) Closed loop configuration
2) open loop configuration.

Open loop configuration

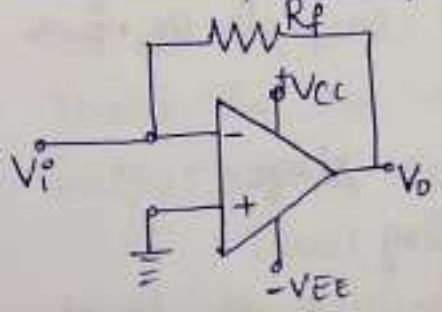


In open loop, there will be no feedback from o/p to i/p. The o/p v/g is given by.

$$V_0 = A_{OL}(V_1 - V_2)$$

A_{OL} is the open loop gain of the Op-Amp.

Closed Loop configuration



The closed loop configuration is as shown in fig. In this, some part of the output is fed back to the i/p through resistor.

* If the feedback is connected to Inverting terminal then it is called Negative feedback.

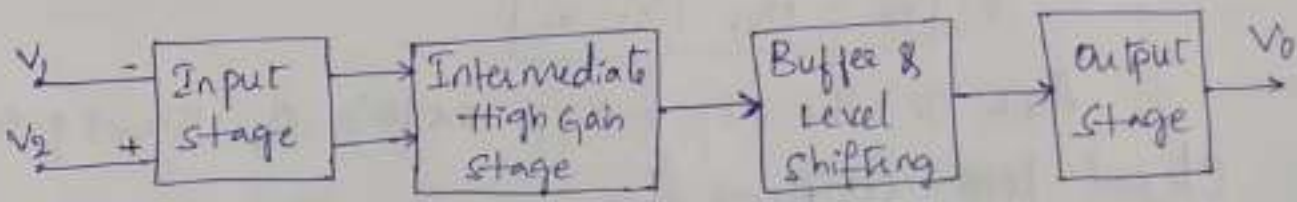
* If the feedback is connected to non-inverting terminal then it is called positive feedback.

* Op-Amp is always used with negative feedback. The gain resulting with feedback is called closed loop gain of the Op-Amp.

Advantages of -ve feedback

1) It reduces the gain and makes it controllable.
2) It reduces the distortion
3) It increases the bandwidth
4) It increases the i/p resistance of the Op-Amp
5) It decreases the o/p resistances of the Op-Amp
6) It reduces the effects of temperature and power supply.

Block Diagram of Op-Amp



Block diagram of Op-Amp consists of four stages
1) Input stage
2) Intermediate High Gain stage
3) Buffer & Level shifting
4) output stage

Input stage: The Op-Amp has two i/p terminals. Its o/p stage requires dual i/p terminals with high gain i/p impedance. These requirements are satisfied by the dual-i/p balanced o/p differential amplifier.

Its function is to amplify the difference b/w the two i/p signals. It provides high differential gain, high i/p impedance and low o/p impedance.

Intermediate High Gain Stage:

The overall gain requirement of an Op-Amp is very high, since the i/p stage alone cannot provide such a high gain. The main function of the intermediate stage is provides such a high gain. It consists of another differential amplifier with dual i/p unbalanced o/p.

practically the intermediate stage is a chain of cascaded amplifiers called as Multistage amplifiers are used.

Buffer And level shifting:

In Op-Amp, because of direct coupling the dc level rises from stage to stage. This increase in dc level tends to shift the operating point of the device used in the next stage. This in turn, limits the o/p voltage swing and may distort the output signal.

Level shifting stage is used bring the dc level to ground potential.

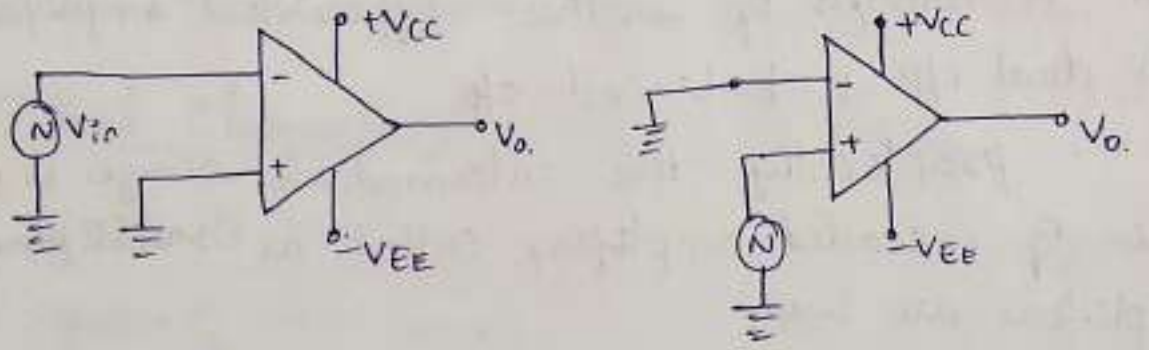
Output stage: The o/p stage requires low o/p impedance, large voltage swing. This is satisfied by class B push pull emitter follower circuit.

Op-Amp Input Modes.

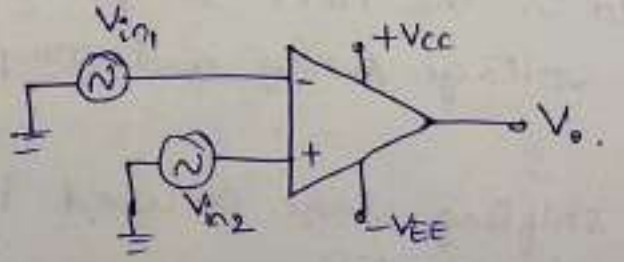
The Op-Amp can be operated in two different modes of input.

1) Differential input mode.
2) Common mode input.
3) Single ended input.

Single ended input: In this mode, the signal voltage is applied to one input and other input grounded. as shown in fig below.



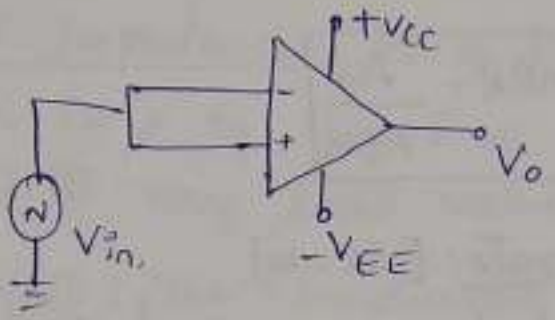
Differential Input: In this mode, 2 out of phase signal voltages are applied to the inputs of the op-amp. This type of operation is also called double ended input operation.



The output is obtained by apply superposition theorem i.e V_{o1} - o/p due to the input V_{in1} only and V_{o2} o/p due to the input V_{in2} only. The total output will be equal to, $V_o = V_{o1} + V_{o2}$.

Common mode input:

In this mode, 2 inphase signal voltages are applied to the input of the op-Amp. i.e



output will be equal to zero since at both the input terminals the same vlg is applied

Ideal Characteristics of an OP-Amp

1. **Infinite Voltage Gain ($A_{OL} = \infty$):** The open loop gain of the amplifier is very large ie infinity
2. **Infinite I/p Impedance:** An ideal Op-Amp does not draw any current from the vlg source connected to its input terminals. Thus its i/p impedance is infinite i.e $Z_{in} = \infty$.
3. **Zero output Impedance:** The output voltage of an ideal op-Amp is independent of the current drawn from it. This means op-amp has zero o/p impedance. i.e $Z_{out} = 0$.

4) Infinite Bandwidth: An ideal op-amp amplifies signals of any frequency with a constant gain. which implies that op-amp has infinite B.W

i.e $\boxed{B.W = \infty}$

5) Infinite CMRR [CMRR = ∞]

CMRR is defined as the ratio of the differential voltage gain to the common mode voltage gain.

i.e $\boxed{CMRR = \frac{A_d}{A_{cm}}}$

6) Infinite Slew rate: [SR = ∞].

An Ideal op-amp has infinite slew rate this implies that the o/p voltage changes simultaneously with the i/p voltages.

7) The characteristics of an ideal op-amp do not change with temperature

8) Zero PSRR [PSRR = 0]:

The power supply Rejection ratio of an ideal op-amp must be equal to zero.

9) Zero offset voltage:

The presence of small o/p vlg when $V_1 = V_2 = 0$ is called an offset voltage.

For an ideal op-amp offset voltage is zero.

Practical Characteristics of Op-Amp

1) Open loop voltage gain : It is the voltage gain of op-amp when no feedback is applied. practically its value is 2×10^5

2) Input impedance: It is typically greater than 1MΩ but using FET [field effect transistor] for input stage it can be increased upto several 100MΩ

3) Output impedance: It is typically few 100Ω with the help of negative feedback it can be reduced to very small value

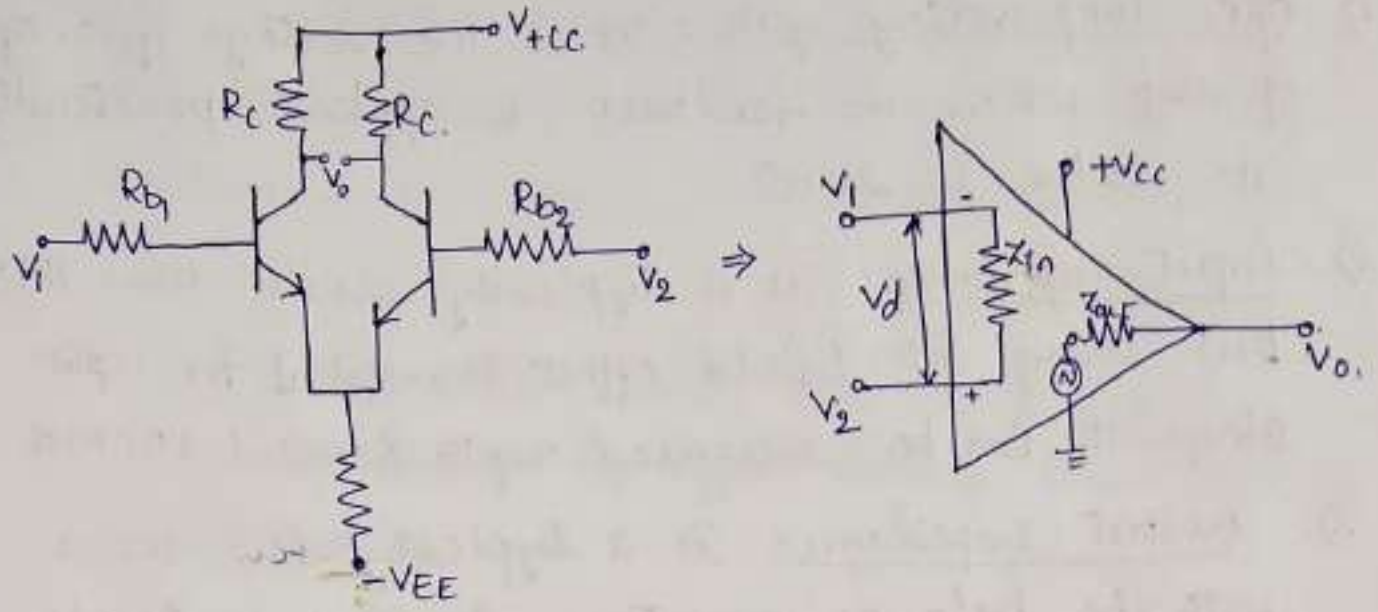
4) Bandwidth : The bandwidth of practical op-amp in open loop configuration is very small by applying feedback it can be increased to desired value. Its range of 1 to 100MHz. typically 1MHz.

5) CMRR (common mode Rejection Ratio): The ratio of differential gain to common mode gain is called CMRR. It is of the order of 90dB.

6) Slew rate: Slew rate ensures that output changes simultaneously with change in input voltage. practical value is 0.5V/μsec.

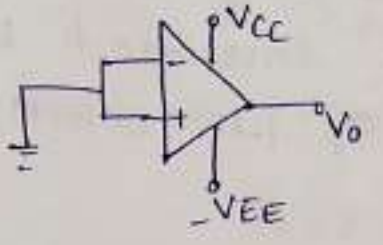
7) PSRR [power supply Rejection Ratio]: It is defined as the ratio of change in input offset v/g to change in power supply v/g keeping other supply constant. The practical value is 30μV/V.

Circuit of an Ideal Op-Amp



Op-Amp Parameters

1) **Offset voltage:** when both the i/p terminals are shorted and connected to ground, the output should be ideally zero. but practically there exist a small dc o/p voltage known as **o/p offset voltage**



To make o/p offset voltage zero, a small voltage is required to be applied to one of the i/p terminals such a voltage makes the output v/g exactly zero. This dc voltage, which makes o/p voltage zero is called **i/p offset voltage.**

For an ideal op-amp both i/p offset v/g and the o/p-offset v/g must be zero i.e offset voltages should be zero.

2) **Power Supply Rejection Ratio:**

PSRR is defined as the ratio of change in input voltage due to change in supply vlg producing it, keeping the other power supply voltage constant.

* If V_{EE} is constant and due to change in V_{CC}, there is change o/p offset voltage then PSRR is expressed as,

$$PSRR = \left.\frac{\Delta V_{IOS}}{\Delta V_{CC}}\right|_{V_{EE}=\text{Constant}}$$

* If V_{CC} is constant & due to change in V_{EE} there is change in o/p offset voltage then PSRR is expressed as,

$$PSRR = \left.\frac{\Delta V_{IOS}}{\Delta V_{EE}}\right|_{V_{CC}=\text{Constant}}$$

3) **CMRR [Common mode Rejection Ratio]**

CMRR is defined as the ratio of the differential Gain [Ad] to the common mode gain [Acm].

$$\boxed{CMRR = \frac{A_d}{A_{cm}}}$$

CMRR is always expressed in Decibels

i.e $$\boxed{CMRR = 20 \log_{10} \frac{A_d}{A_{cm}}}$$

4) **Slew rate:**

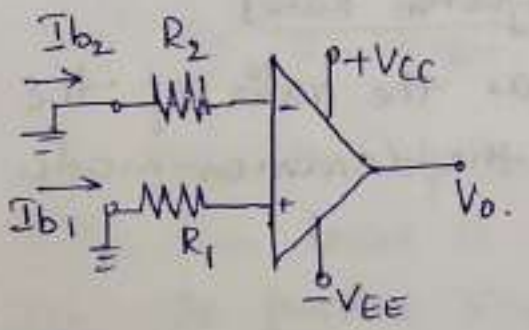
Slew rate of an op-amp is defined as the maximum rate of change of its o/p v/g w.r.t time & is expressed in volts per microsecond.

$$SR = \left.\frac{dV_o}{dt}\right|_{max} \quad V/\mu sec.$$

for 741, $SR = 0.5V/\mu sec.$

Higher the slew rate better the performance of the op-amp. slew rate indicates how fast the o/p of an op-amp can change in response to changes in the input. The slew rate of an op-amp is fixed and if the rate of o/p variation with respect to time is greater than the slew rate, distortion results.

5) **Input bias current**



It is defined as the average value of the individual current flowing into the Inverting and non-inverting i/p terminals of the Op-Amp.

$$I_B = \frac{I_{b_1} + I_{b_2}}{2}$$

Input offset current is the difference b/w the two currents.

$$I_{io} = |I_{b_1} - I_{b_2}|$$

Applications of Op-Amps.

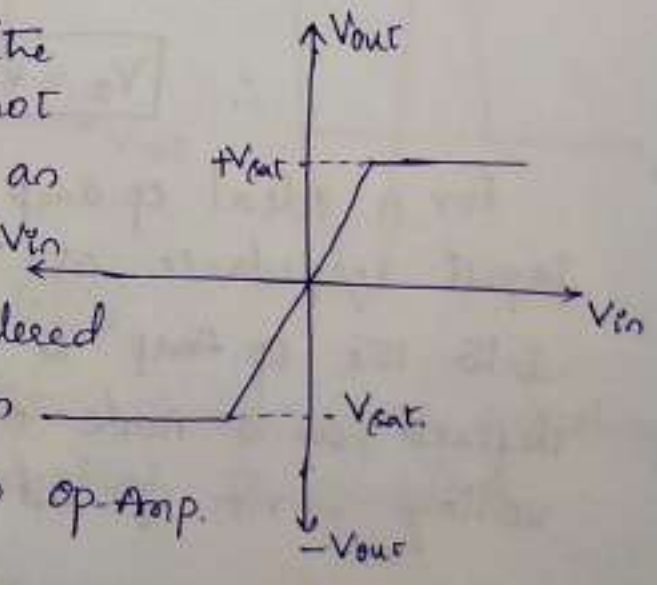
The Op-Amp has numerous applications considering some external resistors and capacitors. Few of the Op-Amp applications are as follows.

1) Inverting Amplifier
2) Non-inverting Amplifier
3) Summer (Adder)
4) Subtractor
5) voltage follower
6) Integrator
7) Differentiator
8) Comparator.

Saturable property of an Op-Amp.

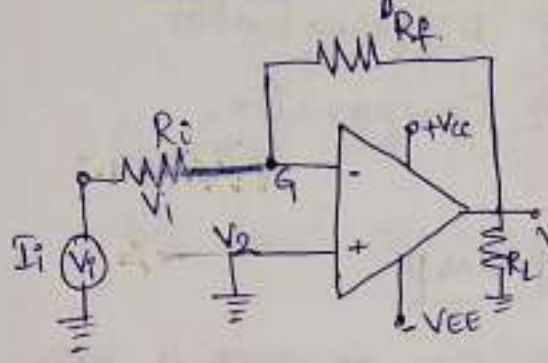
The open loop gain of an op-amp is very high while every op-amp has a property that its output can swing between two levels, decided by the supply voltage is $+V_{CC}$ and $-V_{EE}$. Thus, if output tries to raise more than $+V_{CC}$ & less than $-V_{EE}$ then it gets clipped and gets saturated at the level almost equal to $+V_{CC}$ and $-V_{EE}$ & $+V_{sat}$ and $-V_{sat}$ side respectively.

Once the o/p reaches the saturation level it does not increase further even if an input voltage is increased. The Op-amp is then considered as saturated. This is known as saturable property of an Op-Amp.



The maximum output vlg op-amp & the saturation voltage level are about 90% of the supply levels. Thus for an op-Amp of supply ±12V, the saturation voltage levels are 90% of ±12V i.e ±10.8V.

Concept of Virtual Ground.



The output of an op-Amp is given by

$$V_0 = A \cdot V_{in}$$

$$V_0 = A[V_2 - V_1]$$

$$V_2 - V_1 = \frac{V_0}{A}$$ { A = Gain of the op-Amp.

for an ideal op-Amp, open loop gain = ∞.

$$\therefore V_2 - V_1 = \quad = 0.$$

$$\therefore \boxed{V_2 = V_1}$$

For a ideal op-amp the voltage gain and the input impedance are infinite therefore the current into the op-Amp is zero. The virtual ground is defined as a node & junction that has zero voltage w.r.t ground but it is not physically grounded.

when a non-inverting terminal is grounded, $V_2 = 0$ and V_1 will be at ground potential without actually being grounded. Therefore the node 'G' is called virtual ground and it has zero voltage w.r.t ground.

Since, ideal op-amp has infinite input impedance and because of the concept of virtual ground all the input I_i will pass through feedback resistance R_F and the output voltage V_o is taken across the load resistance R_L.

Applications.

Inverting Amplifier:

Inverting amplifier is a one in which there will be 180° phase shift between the input and output. It is an amplifier which provides a phase difference of 180° in o/p w.r.t i/p.

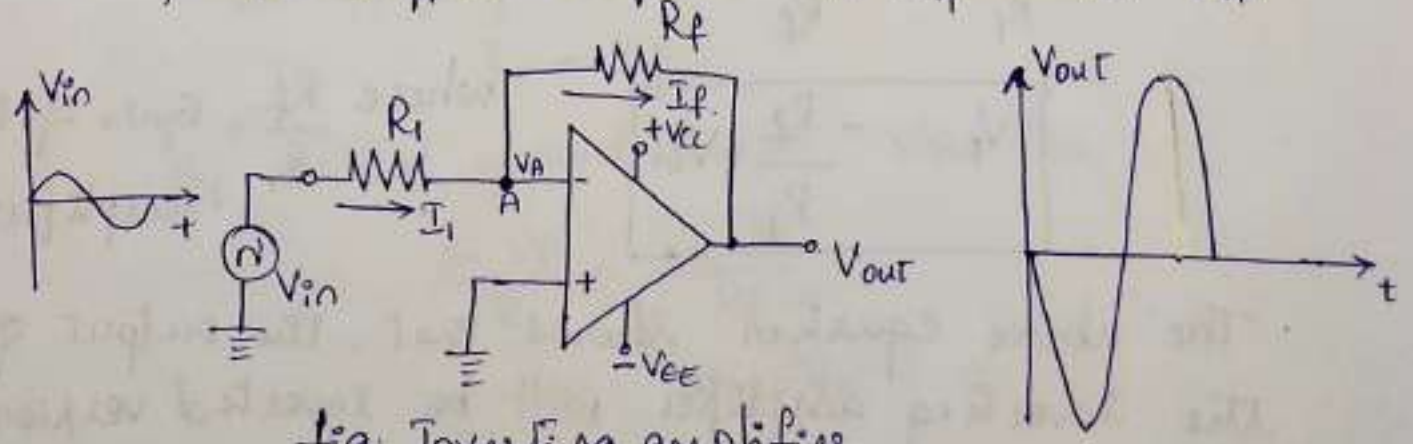


fig: Inverting amplifier.

The above figure shows the circuit of an inverting amplifier. The input V_{in} is applied to inverting

terminal through input resistance R_1. Non-inverting terminal is grounded. R_f is a feedback resistance connected between the input and the output terminal.

Let I_1 be the current through the Resistance R_1 and I_f be the current through the feedback Resistance R_f. According to the virtual ground concept the voltage at node is zero i.e $V_A = 0$. Due to the high i/p impedance of the Op-Amp I_1 will not enter the Op-Amp. So I_1 will flow through the feedback resistor R_f.

$\therefore I_1 = I_f$ [or by applying KCL at node A. i.e current entering the node = current leaving the node].

$$\frac{V_{in} - V_A}{R_1} = \frac{V_A - V_o}{R_f}$$

$$\frac{V_{in} - 0}{R_1} = \frac{0 - V_o}{R_f}$$

$$\boxed{V_o = -\frac{R_f}{R_1} \cdot V_{in}}$$

where $\frac{R_f}{R_1}$ = Gain of the amplifier.

The above equation shows that, the output of the inverting amplifier will be inverted version of the input and V_o is R_f/R_1 times the input signal.

Non-inverting Amplifier

It is an amplifier in which the input signal and the output signals are having phase difference of zero d. Both the input and output will be inphase with each other.

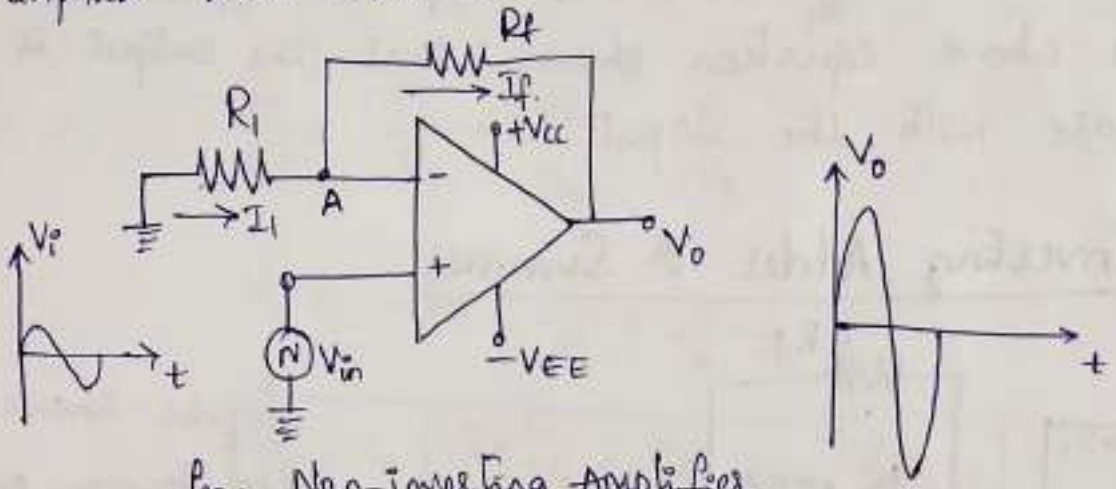


fig: Non-inverting Amplifier

The above figure shows the circuit for a non-inverting amplifier. The input is applied to the non-inverting terminal. Inverting terminal is grounded. R_f is the feedback resistance connected between inverting terminal and the output terminal of op-amp.

On applying KCL at node-A.

$$I_1 = I_f$$

By virtual ground concept, $V_A = V_{in}$.

$$\frac{0 - V_A}{R_1} = \frac{V_A - V_o}{R_f}$$

$$\frac{0 - V_{in}}{R_1} = \frac{V_{in} - V_o}{R_f}$$

$$\frac{V_o}{R_f} = V_{in}\left[\frac{1}{R_1} + \frac{1}{R_f}\right]$$

$$V_0 = V_{in} \cdot R_f \left[\frac{1}{R_1} + \frac{1}{R_f}\right]$$

$$\boxed{V_0 = \left[1 + \frac{R_f}{R_1}\right] \cdot V_{in}} \rightarrow$$ Expression for o/p of an Non-inverting amplifier

where $1 + \frac{R_f}{R_1}$ is the Gain of the amplifier. and the above equation shows that the output is in phase with the input.

Inverting Adder & Summer.

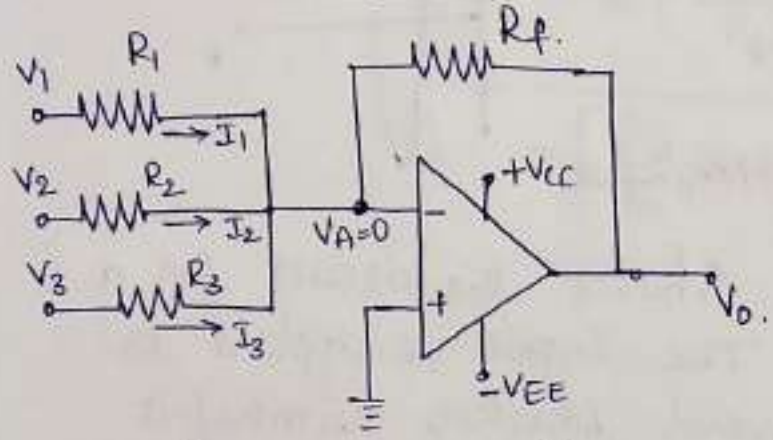


fig: Inverting Adder using op-Amp.

figure shows the ckt diagram of the Inverting adder. where V_0 is the output voltage which is the sum of input voltages applied at the inverting input terminal.

V_1, V_2 & V_3 are the inputs applied through resistances R_1, R_2 & R_3 respectively. The feedback resistance R_f is connected blw the inverting and the output terminal. Non-inverting terminal is grounded. Since, input impedance of the op-Amp is very high & infinite, no current flows through the op-Amp.

let I_1, I_2 & I_3 are the current through R_1, R_2 & R_3 respectively.

On applying KCL to the ckt

$$I_f = I_1 + I_2 + I_3.$$

$$\frac{0 - V_o}{R_f} = \frac{V_1 - 0}{R_1} + \frac{V_2 - 0}{R_2} + \frac{V_3 - 0}{R_3}$$

$$\frac{-V_o}{R_f} = \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}$$

$$V_o = -R_f \left[\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right]$$

$$\boxed{V_o = -\left[\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3 \right]} \longrightarrow (1)$$

let $R_1 = R_2 = R_3 = R_f = R$

$$V_o = -\left[\frac{R}{R} V_1 + \frac{R}{R} V_2 + \frac{R}{R} \right]$$

$$\boxed{V_o = -[V_1 + V_2 + V_3]} \longrightarrow (2)$$

if $R_1 = R_2 = R_3 = R$

$$\boxed{V_o = -\frac{R_f}{R}[V_1 + V_2 + V_3]} \longrightarrow (3)$$

The above equations (1) & (2) & (3) shows that output voltage is the sum of all the input voltages.

Non-Inverting Adder

In non-inverting adder, the input voltage V_1 & V_2 are appled to a non-inverting terminal through resistor R_1 & R_2 respectively. and Inverting terminal is grounded. R_f is the feedback resistor connected blw o/p terminal and inverting terminal.

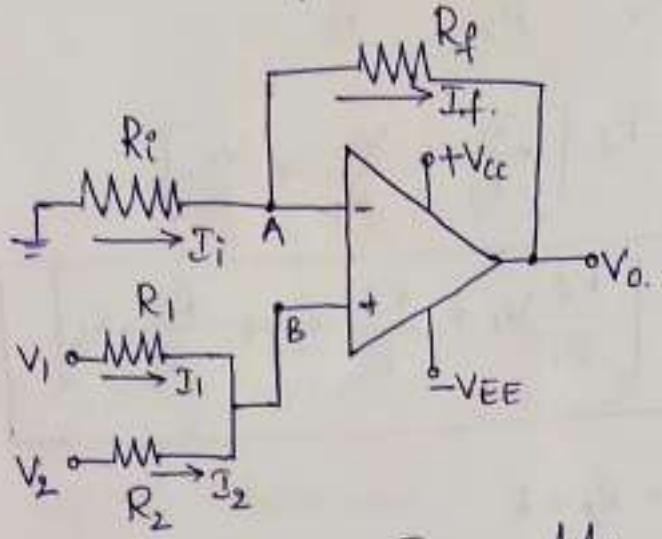


fig: Non-inverting adder using Op-Amp.

from the fig: $I_1 + I_2 = 0$ [∵ due to high i/p impedance no current flows into Op Amp]

$$\frac{V_1 - V_B}{R_1} + \frac{V_2 - V_B}{R_2} = 0.$$

$$\frac{V_1}{R_1} - \frac{V_B}{R_1} + \frac{V_2}{R_2} - \frac{V_B}{R_2} = 0$$

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} = V_B\left[\frac{1}{R_1} + \frac{1}{R_2}\right]$$

$$\frac{V_1 R_2 + V_2 R_1}{R_1 R_2} = V_B\left[\frac{R_2 + R_1}{R_1 R_2}\right]$$

$$\boxed{V_B = \frac{V_1 R_2 + V_2 R_1}{R_1 + R_2}} \rightarrow (1)$$

At node A,

$$I_i = I_f$$

$$\frac{0 - V_A}{R_i} = \frac{V_A - V_o}{R_f}$$

$$-\frac{V_A}{R_i} = \frac{V_A}{R_f} - \frac{V_o}{R_f}$$

$$\frac{V_o}{R_f} = V_A\left[\frac{1}{R_i} + \frac{1}{R_f}\right]$$

$$\boxed{V_o = V_A\left[\frac{R_f}{R_i} + 1\right]} \longrightarrow (2)$$

According virtual ground concept. $V_A = V_B$.

$\therefore$ eq-(2) becomes

$$V_o = V_B\left[\frac{R_f}{R_i} + 1\right]$$

from eq-(1) we have $V_B = \frac{V_1 R_2 + V_2 R_1}{R_1 + R_2}$

$$\boxed{V_o = \left[\frac{V_1 R_2 + V_2 R_1}{R_1 + R_2}\right]\left[1 + \frac{R_f}{R_i}\right]}$$

Let $R_1 = R_2 = R_i = R_f = R$

$$\therefore V_o = \left[\frac{V_1 R + V_2 R}{R + R}\right]\left[1 + \frac{R}{R}\right]$$

$$= \left[\frac{V_1 + V_2}{2R}\right] \cdot R \left[1 + 1\right]$$

$$\boxed{V_o = V_1 + V_2}$$ → This shows that the o/p is the sum of i/ps V_1 & V_2

Subtractor [Difference Amplifier]

The circuit is designed using Op-Amp such that its output voltage is difference between two input voltages & Subtraction of two input voltages is called Subtractor & Difference Amplifier.

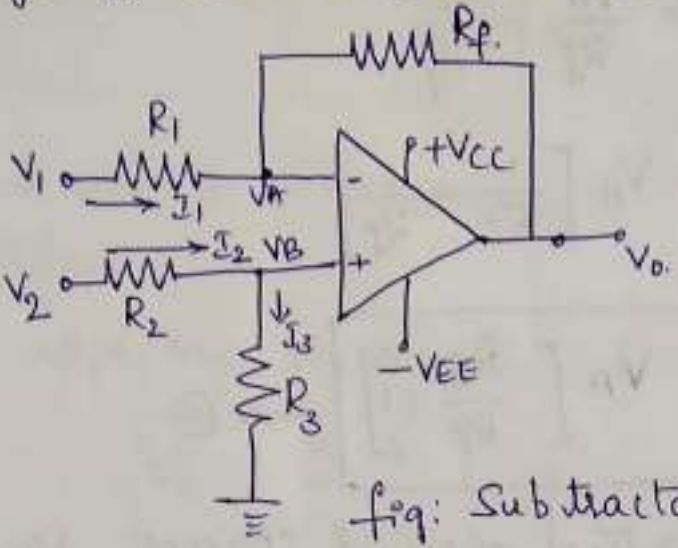


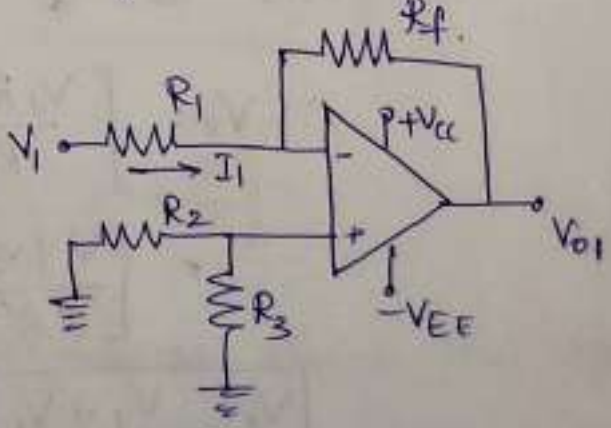
fig: Subtractor & Difference Amplifier.

figure shows the Subtractor ckt. using Op-Amp. Rf is the feedback resistor connected b/w Inverting terminal and output terminal of the Op-Amp.

To determine the output voltage of Subtractor, the principle of Superposition-theorem is used.

Case 1) An input voltage V_1 is applied and $V_2 = 0$. i.e grounding the non-inverting terminal then the respective output is V_{01}

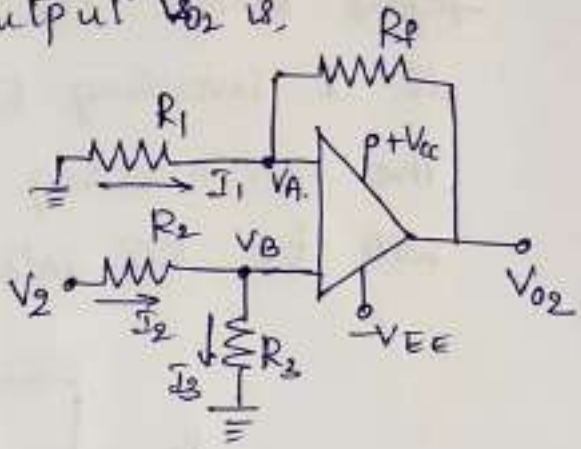
$$V_{01} = \frac{-R_f}{R_1} \cdot V_1 \rightarrow (1)$$



The circuit is in Inverting Amplifier.

Case 2) when input terminal V_1 is grounded and i/p voltage is applied to V_2 on grounding inverting terminal and the respective output V_{O2} is,

$$V_{O2} = V_B \left[1 + \frac{R_f}{R_1}\right] \rightarrow (2)$$



The circuit is non-inverting amplifier.

By applying Vlg divider rule, at node B.

$$V_B = \frac{V_2 \cdot R_3}{R_2 + R_3} \rightarrow (3).$$

On substituting (3) in (2).

$$V_{O2} = \frac{V_2 \cdot R_3}{R_2 + R_3}\left[1 + \frac{R_f}{R_1}\right]$$

Therefore, the total output voltage,

$$V_O = V_{O1} + V_{O2}$$

$$V_O = -\frac{R_f}{R_1} \cdot V_1 + \frac{V_2 \cdot R_3}{R_2 + R_3}\left[1 + \frac{R_f}{R_1}\right]$$

let $R_1 = R_2 = R_3 = R_f = R$

$$V_O = -\frac{R}{R} \cdot V_1 + \frac{V_2 \cdot R}{R+R}\left[1 + \frac{R}{R}\right]$$

$$\boxed{V_O = V_2 - V_1} \rightarrow$$ This expression shows that o/p is the difference b/w two input voltages

Integrator:

The circuit of an Integrator is as shown in figure below. The input voltage V_i is applied to a inverting terminal through resistance R. The non inverting terminal is grounded. The o/p will be the integration of the i/p voltage.

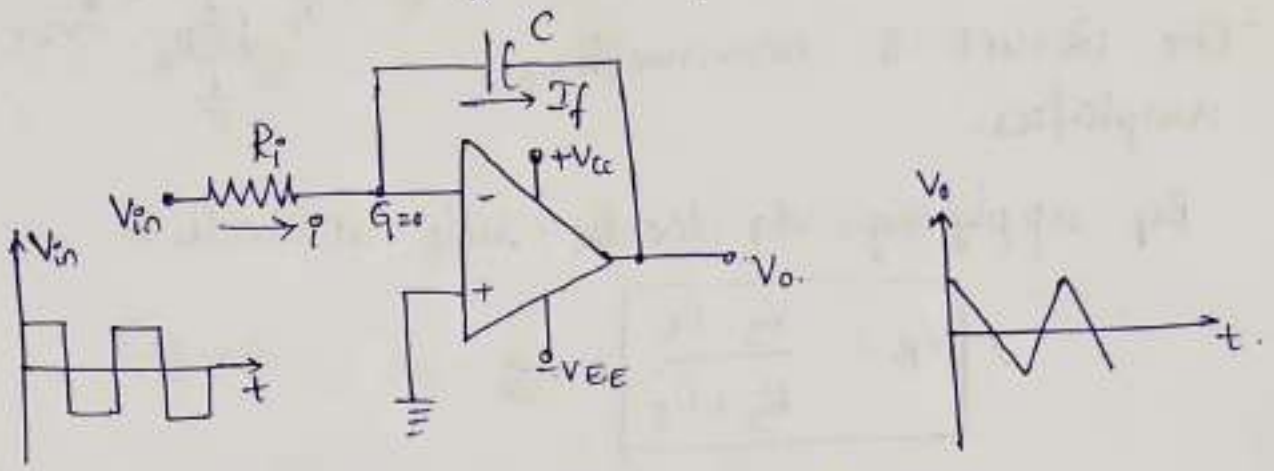


fig: Integrator using Op-Amp.

Capacitor C is connected blw output terminal and inverting terminal. G is the virtual ground. Since Input Impedance of op-Amp is infinite, no current will flow through op-Amp. All the current flows through capacitor.

The input V_i charges the capacitor to a voltage V_o. Charge on the capacitor is given by.

$$q = CV.$$

$$q = C[V_G - V_o]$$

$$\boxed{q = -CV_o} \rightarrow (1) \quad [\because V_G = 0]$$

we know that,

$$q = \int_0^t i \cdot dt \longrightarrow (2)$$

$$i = \frac{V_{in} - V_G}{R}$$

$$i = \frac{V_{in}}{R}$$

$$\therefore q = \int_0^t \frac{V_{in}}{R} \cdot dt. \longrightarrow (3).$$

$$q = \frac{1}{R} \int_0^t V_{in} \cdot dt. \longrightarrow (4)$$

Equating eq-(4) & (1)

$$-CV_0 = \frac{1}{R} \int_0^t V_{in} \cdot dt$$

$$\boxed{V_0 = \frac{-1}{RC} \int_0^t V_{in} \cdot dt} \longrightarrow (5)$$

Eq-(5) shows that output is the integral of input. RC represents the time constant.

Integrator input	integrator o/p.
Square wave	Triangular wave
Step input	Ramp output
Sine wave	Cosine wave.

Differentiator:

In a Differentiator circuit show below, input voltage V_i is applied to inverting terminal through a capacitor C. The non-inverting terminal is grounded. R_f is the feedback resistor connected blw the o/p terminal and inverting-terminal. G. is a virtual ground [$V_G = 0$]. Since input impedance of the op-amp is infinite, no current flows through it and all current flows through feedback resistor R_f.

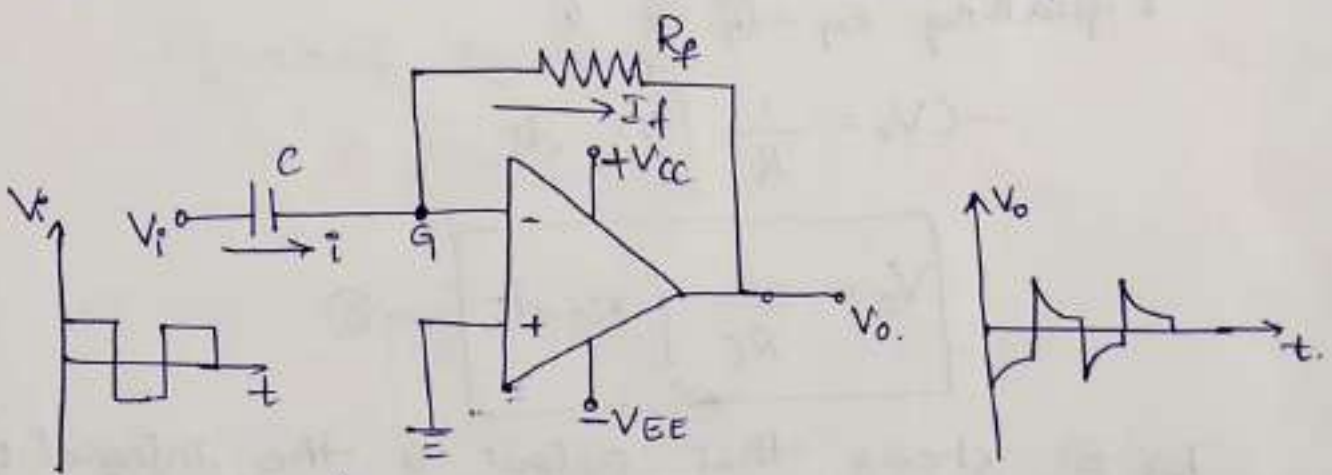


fig: Differentiator using Op-Amp.

The charge on the capacitor is given by.

$$q = CV$$
$$= C[V_{in} - V_G]$$
$$\therefore q = CV_{in}$$
$$\therefore V_{in} = \frac{q}{C} \longrightarrow (1).$$

differentiating eq (1) w.r.t t

$$\frac{dv_{in}}{dt} = \frac{1}{C}\frac{dq}{dt}$$

$$C \cdot \frac{dV_{in}}{dt} = \frac{dq}{dt} \longrightarrow (2).$$

W.K.T $\quad q = \int_0^t i \cdot dt \Rightarrow \frac{dq}{dt} = i.$

from the ckt,

$$i = I_f$$

$$I_f = \frac{V_G - V_o}{R}$$

$$i = \frac{-V_o}{R}$$

$$\frac{dq}{dt} = \frac{-V_o}{R} \longrightarrow (3).$$

Equating eq ③ & ②

$$C \cdot \frac{dV_{in}}{dt} = -\frac{V_o}{R}$$

$$\boxed{V_o = -RC \frac{dV_{in}}{dt}} \longrightarrow (4).$$

The above equation represents that output of differentiator circuit is the differentiation of the input.

Comparators:

Op-Amps are often used as comparators to compare the amplitude of one voltage with another. In this application, the Op-Amps is used in open loop configuration (i.e no feedback) with input voltage on one input and the reference

Voltage on the other.

Consider the ckt, shown in fig below with input voltage V_{in}

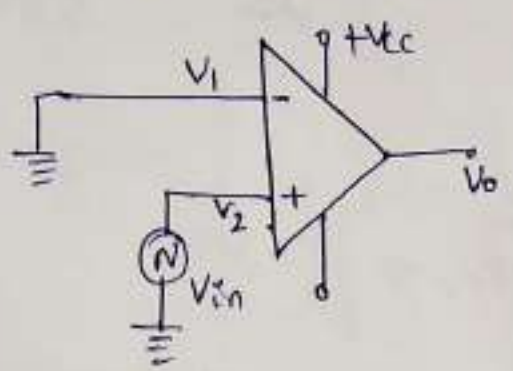


fig: comparator ckt.

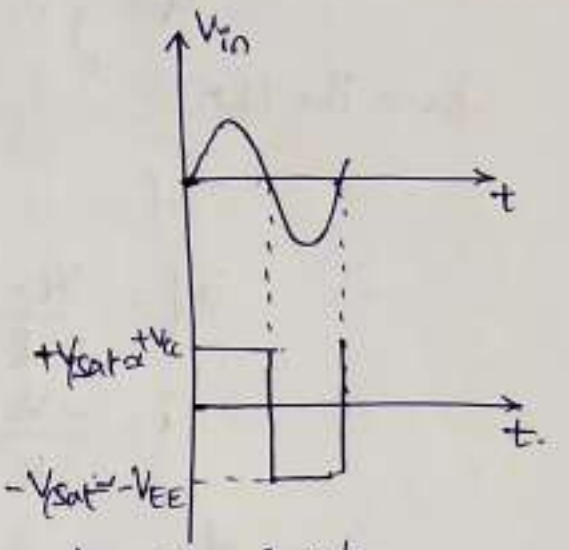


fig: i/p & o/p.

$V_2 = V_{in}$ & $V_1 = 0$.

when $V_{in} > V_1$ i.e $V_{in} > 0$ $\quad V_0 = V_{sat} \simeq +V_{cc}$

when $V_{in} < V_1$ i.e $V_{in} < 0$ $\quad V_0 = -V_{sat} \simeq -V_{EE}$

The above circuit is also called zero-crossing Detector

Formulae

1) $CMRR = \frac{|Ad|}{|Acm|}$

$CMRR \text{ in dB} = 20 \log \frac{Ad}{Acm}$.

2) Gain of Non-inverting Amplifier

$Af = 1 + \frac{Rf}{R_1}$

3) Gain of Inverting, $Af = -\frac{Rf}{R_1}$

4) Inverting Summer, $V_0 = -\left[\frac{Rf}{R_1}V_1 + \frac{Rf}{R_2}V_2 + \frac{Rf}{R_3}V_3\right]$

8) Non-inverting Adder.

$$V_0 = V_B\left[1 + \frac{R_f}{R_1}\right]$$

$$V_B\left[\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right] = \left[\frac{1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right]$$

9) Integrator :

$$V_0 = \frac{-1}{R_C}\int_0^t V_{in}\, dt$$

10) Differentiator :

$$V_0 = -R_C \frac{dV_{in}}{dt}$$

11) Input offset current.

$$I_{io} = |I_{b1} - I_{b2}|$$

12) Input bias current

$$I_B = \frac{I_{b1} + I_{b2}}{2}$$

Problems:

1. If the base current for the transistor of a transistor of a differential amplifier 8μA and 12 μA. Determine a) Input bias current
b) Input offset current.

Given: $I_{b1} = 8\mu A$ $I_{b2} = 8\mu A$.

$$I_B = \frac{I_{b1} + I_{b2}}{2} = \frac{(8+12)\times 10^{-6}}{2} = 10\mu A.$$

Input offset current = $|I_{b1} - I_{b2}| = |8-12|$

$$\boxed{I_{io} = 4\mu A}$$

2) For a practical op-amp, while input bias current is 60nA and input offset current 20nA. Calculate the value of two input bias current.

Given: $I_B = 60nA$. $\quad I_{b1} - I_{b2} = 20nA. \rightarrow (1)$

$$I_B = \frac{I_{b1} + I_{b2}}{2}$$

$$60nA = \frac{I_{b1} + I_{b2}}{2} \quad \therefore I_{b1} + I_{b2} = 120nA. \rightarrow (2)$$

Solving eq-(1) & (2)

$2I_{b1} = 140nA$ $\quad -2I_{b2} = -100nA.$

$\boxed{I_{b1} = 70nA}$ $\quad \boxed{I_{b2} = 50nA}$

3). Determine the input bias current and input offset current to an op-amp if the current into non-inverting & inverting terminals are 8.3μA & 7.9μA respectively.

Soln: Given: $I_{b1} = 7.9\mu A \quad I_{b2} = 8.3\mu A.$

$$I_B = \frac{I_{b1} + I_{b2}}{2} = \frac{(7.9 + 8.3)\mu A}{2}$$

$\boxed{I_B = 8.1\mu A.}$

$$I_{io} = |I_{b1} - I_{b2}|$$

$$= |7.9 - 8.3|$$

$\boxed{I_{io} = 0.4\mu A}$

4) A certain op-amp has a differential vlg gain of 1,00,000 and common-mode gain of 0.25. Determine the CMRR and express it in decibles.

Given: $A_d = 100000$ $A_{cm} = 0.25$

$$CMRR = \frac{A_d}{A_{cm}} = \frac{100000}{0.25} = 4,00,000$$

$$CMRR = 20 \log_{10} \frac{A_d}{A_{cm}}$$

$$\boxed{CMRR = 112.04 \text{ dB}}$$

5) An op-amp has a differential vlg gain of 2500 and a CMRR of 30000

a) Determine the common mode gain

b) Express the CMRR in dB.

Soln: Given: $A_d = 2500$, $CMRR = 30000$

a) $$CMRR = \frac{A_d}{A_{cm}}$$

$$A_{cm} = \frac{A_d}{CMRR} = \frac{2500}{30000}$$

$$A_{cm} = 0.083$$

b) CMRR in decibels $= 20 \log_{10}(30000)$

$= 89.54$ dB.

6) When a pulse is applied to an op-Amp the o/p vlg change from $-8V$ to $+7V$ in 0.75 μs. What is

the slew rate?

$$\text{slew rate} = \left.\frac{dV_o}{dt}\right|_{max}$$

$$= \frac{7-(-8)}{0.75}$$

$$\boxed{S.R = 20V/\mu s}$$

⇒ How long does it take the o/p v/g of an op-amp to go from −10V to +10V, if the slew rate is 0.5V/μs

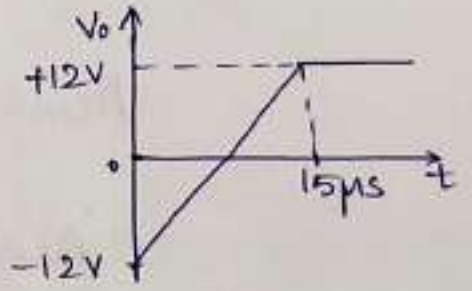
Given: $SR = 0.5V/\mu s$, $dV_o = +(0-(-10)) = 20$.

$$\text{slew rate} = \left.\frac{dV_o}{dt}\right|_{max}$$

$$dt = \frac{10-(-10)}{0.5}$$

$$\boxed{dt = 40\mu s}$$

8) Below shows the o/p v/g V_o of an op-Amp in response to a step i/p. what is the S.R.



Given: from the fig.

$$dV_o = +12-(-12V)$$

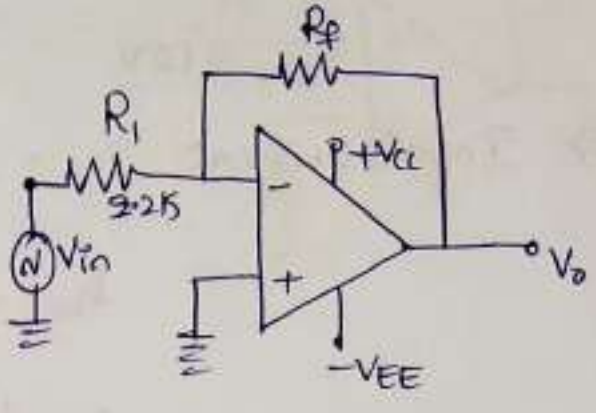
$$= 24V$$

$$dt = 15\mu s.$$

$$S.R = \left.\frac{dV_o}{dt}\right|_{max} = \frac{\text{difference in o/p v/g}}{\text{Difference in time.}}$$

$$S.R = \frac{24}{15\,\mu s} = 1.6V/\mu s$$

9) Given op-amp circuit shown in fig. determine the value of R_f required to obtain a closed loop v/g gain of -50.



Soln: The circuit is inverting amplifier

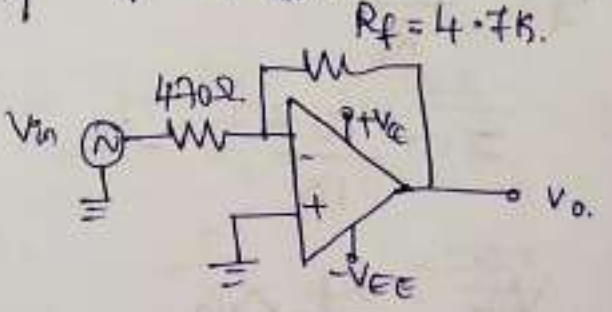
$$\therefore V_o = -\frac{R_f}{R_1} \cdot V_{in}$$

$$\text{Gain} = -\frac{R_f}{R_1} \qquad \text{gain} = -50 \text{ dB}.$$

$$R_f = -(-50) \times 2.2\,K$$

$$\boxed{R_f = 110\,K\Omega.}$$

10) For the inverting amplifier shown in fig. Calculate the values of A_f & R_{in}



$$V_o = -\frac{R_f}{R_1} \cdot V_{in}$$

$$\text{Gain} = \frac{-R_f}{R_1}$$

$$= \frac{4.7K.}{470\,\Omega} \qquad \text{Gain} = A_f = -10.$$

11) For the circuit of inverting amplifier $R_f = 100K\Omega$, $R_1 = 10K\Omega$, and $V_{in} = 1V$. Calculate.

1) closed loop gain, A_v 2) o/p v/g, V_o.

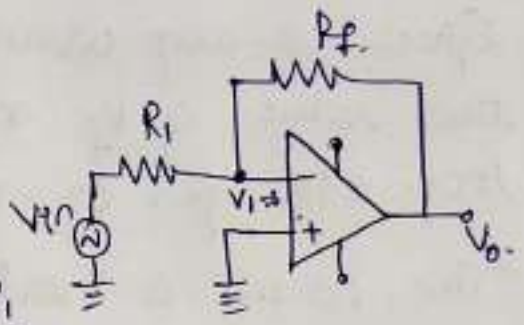
3) Input current I_{in} 4) Feedback current I_f

Soln: 1) $\text{Gain} = A_v = \frac{-R_f}{R_1} = \frac{-100K}{10K} = -10$.

2) o/p v/g $V_0 = A_f \cdot V_{in}$

$= -10 \times 1V.$

$V_0 = -10V.$



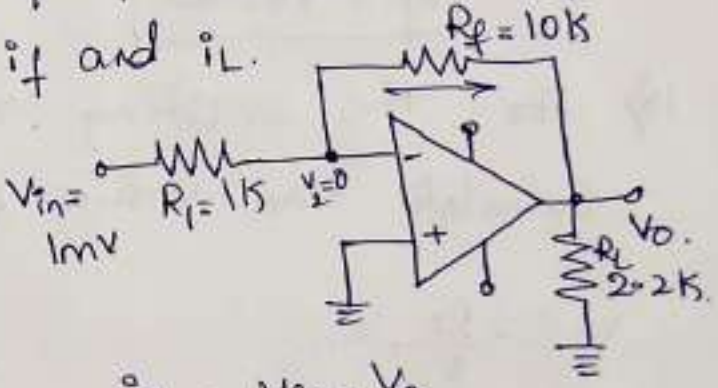
3) Input Current $I_{in} = \frac{V_{in} - V_1}{R_1}$

$I_{in} = \frac{V_{in}}{R_1}$

$= \frac{1}{10 \times 10^3} = 0.1mA.$

4) feedback current. $I_f = i_{in} = 0.1mA.$

12) For the inverting amplifier shown in fig. determine A_f, V_0, i_{in}. i_f and i_L.



$A_f = \frac{-R_f}{R_1}$

$= -\frac{10K}{1K} = -10.$

$V_0 = -\frac{R_f}{R_1} \times V_{in}$

$= \frac{-10K}{1K} \times 1mV.$

$\boxed{V_0 = -10mV}$

$i_{in} = \frac{V_{in} - V_2}{R_1}$

$= \frac{1mV}{1K}$

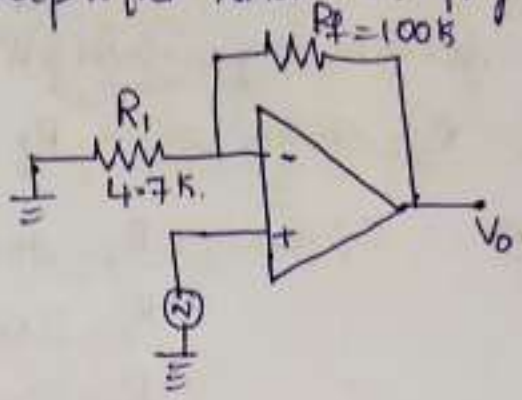
$\boxed{i_{in} = 1mA}$

$i_f = \frac{V_2 - V_0}{R_f}$ & $\boxed{i_f = i_{in} = 1A}$

Load current $i_L = \frac{-V_0}{R_L} = \frac{-10}{2.2 \times 10^3}$

$\boxed{i_L = -4.55mA}$

13). Determine the gain of the amplifier shown in fig



Soln:

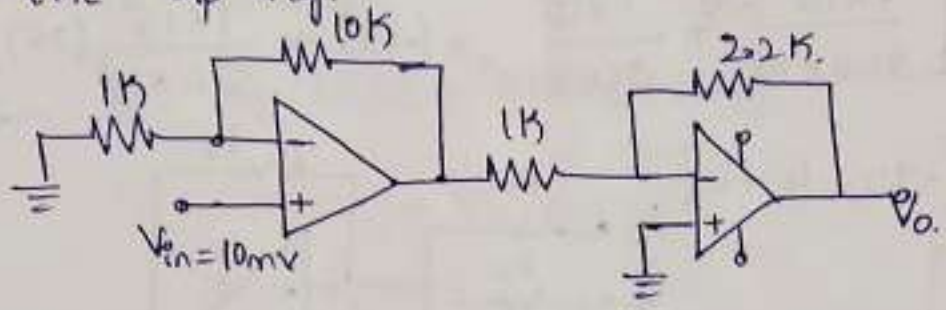
$$V_o = \left[1 + \frac{R_f}{R_1}\right] V_{in}.$$

$$A = 1 + \frac{R_f}{R_1}$$

$$= 1 + \frac{100K}{4.7K}$$

$$\boxed{A = 22.3}$$

14). For the Cascade amplifier shown in fig. determine the o/p v/g.



Soln: A_1 = Gain of the 1st stage $= 1 + \frac{R_f}{R_1} = 1 + \frac{10K}{1K} = 11.$

A_2 = Gain of the 2nd stage $= -\frac{R_f}{R_1} = -\frac{2.2K}{1K}$

∴ Gain of the overall circuit $= -2.2.$

$$A_f = A_1 \cdot A_2$$

$$= 11 \cdot (-2.2) = -24.2.$$

∴ output v/g = $V_o = A_f \cdot V_{in}$

$$= (-24.2)(10 \times 10^{-3})$$

$$\boxed{V_o = -242\ mV}$$

16) Calculate the o/p v/g of a three inverting summing amplifier given: $R_1 = 800K$, $R_2 = 250K$, $R_3 = 500K\Omega$, $R_f = 1M\Omega$, $V_1 = -2V$, $V_2 = -1V$, $V_3 = 3V$

Soln: Given: $R_1 = 800K\Omega$, $V_1 = -2V$

$R_2 = 250K\Omega$, $V_2 = -1V$, $R_f = 1M$.

$R_3 = 500K\Omega$, $V_3 = 3V$

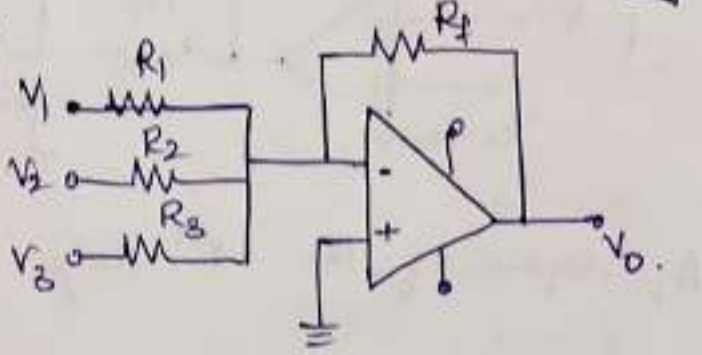
O/p of the Inverting Amplifier

$$V_o = -\left[\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right]$$

$$= -\left[\frac{1\times10^6}{800\times10^3}(-2V) + \frac{1\times10^6}{250\times10^3}\times(-1V) + \frac{1\times10^6}{500\times10^3}(3V)\right]$$

$$= -[-10 - 4 + 6]$$

$$\boxed{V_o = 8V}$$



17) Design an adder circuit using op Amp to obtain an o/p voltage of $V_o = -[2V_1 + 3V_2 + 5V_3]$. where V_1 & V_2 & V_3 are input voltage. Draw the circuit diagram.

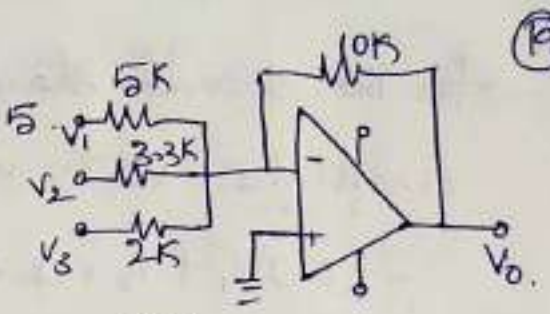
Soln: $$V_o = 2V_1 + 3V_2 + 5V_3 \rightarrow (1)$$

The o/p expression for adder ckt is

$$V_o = -\left[\frac{R_f}{R_1}.V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}.V_3\right] \rightarrow (2)$$

Comparing (1) & (2)

$\frac{R_f}{R_1} = 2$ $\quad \frac{R_f}{R_2} = 3$ $\quad \frac{R_f}{R_3} = 5$



let $R_f = 10K\Omega$.

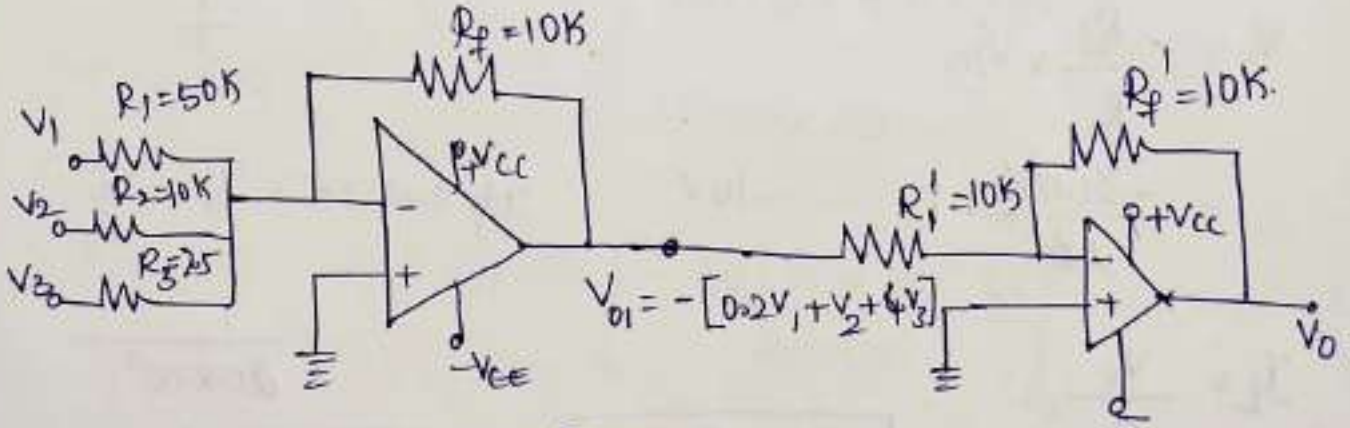
$R_1 = \frac{10K}{2} = 5K$ $\quad R_3 = \frac{10K}{5}$

$R_2 = \frac{10K}{3} = 3.3K$ $\quad \boxed{R_3 = 2K}$

18) Design an adder circuit using Op-Amp to obtain an o/p vtg eq $V_0 = 2[0.1V_1 + 0.5V_2 + 2V_3]$ where V_1, V_2 & V_3 are input voltages. Draw the circuit diagram.

Soln: $V_0 = 2[0.1V_1 + 0.5V_2 + 2V_3]$

$V_0 = 0.2V_1 + V_2 + 4V_3$.



inverting.

$V_0 = 0.2V_1 + V_2 + 4V_3$

let us design a ↑ summer with $V_0 = -[0.2V_1 + V_2 + 4V_3]$.

then use amplifier with unity gain.

$V_0 = [0.2V_1 + V_2 + 4V_3] = -\left[\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right]$

$\frac{R_f}{R_1} = 0.2$ $\quad \frac{R_f}{R_2} = 1$ $\quad \frac{R_f}{R_3} = 4$ $\quad$ let $R_f = 10K$.

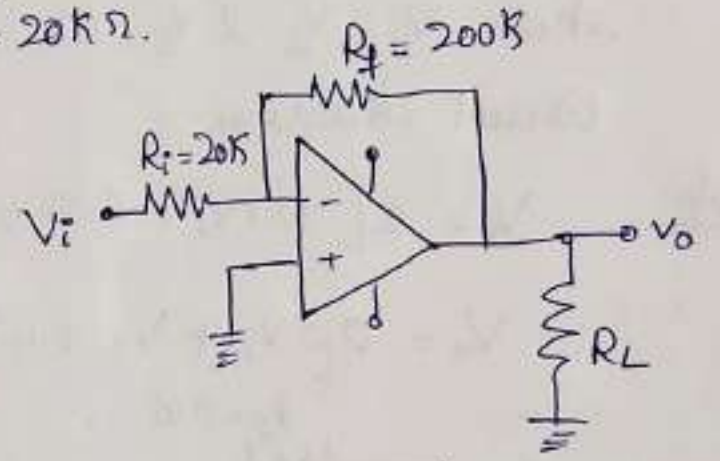
$\therefore$ $\boxed{R_1 = 50K}$ $\quad \boxed{R_2 = 10K}$ $\quad \boxed{R_3 = 2.5K\Omega}$

for the second stage we will use inverting amplifier with unity gain to convert

$-[0.2V_1 + V_2 + 4V_3]$ to $[0.2V_1 + V_2 + 4V_3]$.

$$\therefore \frac{R_f'}{R_1'} = 1 \Rightarrow \underline{R_f' = R_1 = 10K.}$$

19) An inverting amplifier has load resistance of 50KΩ connected to its o/p. If $V_i = 1V$. find load current, o/p v/g and i/p current if $R_f = 200K\Omega$ $R_i = 20K\Omega$.



Given: $R_L = 50K\Omega$, $V_i = 1V$

$R_f = 200K\Omega$.

$$V_o = -\frac{R_f}{R_1} \times V_{in}$$

$$= \frac{-200K}{20K} \cdot 1V = -10V.$$

I/p current = $I_i = \frac{V_i}{R_i}$

$$= \frac{1}{20 \times 10^3}$$

$\boxed{I_i = 50\mu A}$

$$I_L = \frac{V_o}{R_L}$$

$$= \frac{-10V}{50K}$$

$\Rightarrow \boxed{I_L = -0.2mA}$

20). A Sinusoidal with peak value of 6mv and 2KHz frequency is applied to the i/p of an ideal op-amp integrator with $R_1 = 100K\Omega$ and $C_1 = 1\mu F$ Find the o/p v/g.

Given $R_1 = 100K\Omega$, $f = 2KHz$, $C = 1\mu F$

$V_m = 6mV = 6\times10^{-3}V$ $\omega = 2\pi f = 2\pi\times2\times10^3$

$V_{in} = 6\times10^{-3}\sin(4\pi\times10^3 t)$ $= 4\pi\times10^3$ rad/s.

Soln: The o/p v/g of the integrator is given by

$$V_0 = \frac{-1}{RC}\int_0^t V_{in}\,dt$$

$$= \frac{-1}{100\times10^3\times1\times10^{-6}}\int_0^t 6\times10^{-3}\sin(4\pi\times10^3 t)$$

$$= \frac{-6\times10^{-3}}{100\times10^3\times1\times10^{-6}}\int_0^t \sin(4\pi\times10^3 t)$$

$$= -0.06\int_0^t \sin(4\pi\times10^3 t)\,dt$$

w.k.t $\int \sin a\theta = -\frac{\cos a\theta}{a}$

$$= -0.06\left[\frac{-\cos(4\pi\times10^3 t)}{4\pi\times10^3}\right]_0^t$$

$$= \frac{-0.06}{4\pi\times10^3}\left[-\cos(4\pi\times10^3 t) - \cos(0)\right]$$

$$\boxed{V_0 = 4.77\times10^{-6}\left[\cos(4\pi\times10^3 t) - 1\right]}$$

(21) In a basic differentiator circuit, the input is a sine wave with peak to peak amplitude of 3V at 200Hz. Determine the o/p v/g. Given time constant $R_f C_1 = 0.15$ msec.

Given: $R_f C_1 = 0.15$ msec, $f = 200$ Hz.

$$\omega = 2\pi f = 2\pi \times 50 = 400 \text{ rad/sec}$$

$$V_{in} = 1.5 \sin 400\,t \quad [\because V_{in} = V_m \sin \omega t]$$

$V_m = 1.5$V.

$$V_0 = -R_f C_1 \frac{dv_{in}}{dt}$$

$$= -0.15 \times 10^{-3} \times \frac{d}{dt}[1.5 \sin 400.\,t]$$

$$= -0.15 \times 10^{-3} \times 1.5 \times 400 \cos 400\,t.$$

$$\therefore \boxed{\text{o/p v/g} = V_0 = -0.283 \cos 400\,t \text{ V}}$$

MODULE-4

BJT Applications, Feedback Amplifiers and Oscillators

BJT as an Amplifier

Amplification: It is the process of increasing & raising the strength of the weak signals.

Generally BJT can be used as current amplifier.

i.e $\boxed{\beta = \frac{I_C}{I_B}}$ → Current Amplification factor [DC].

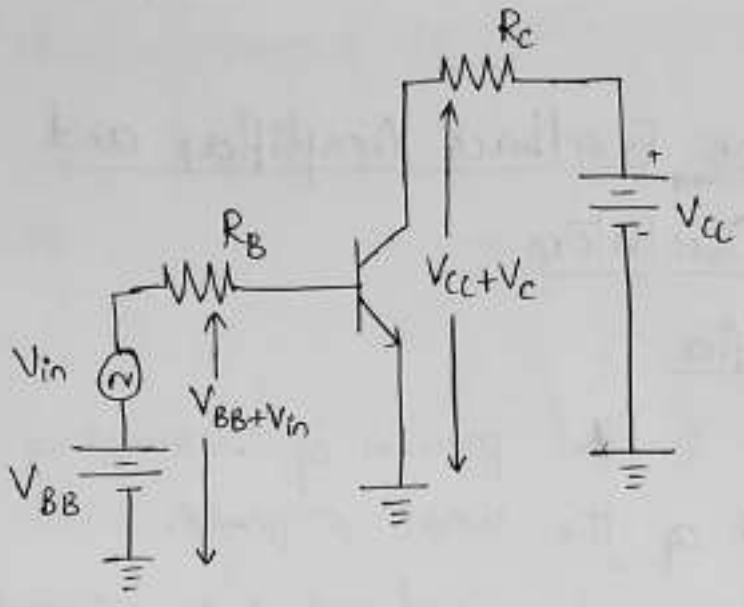
And we also have $I_E = I_C + I_B$

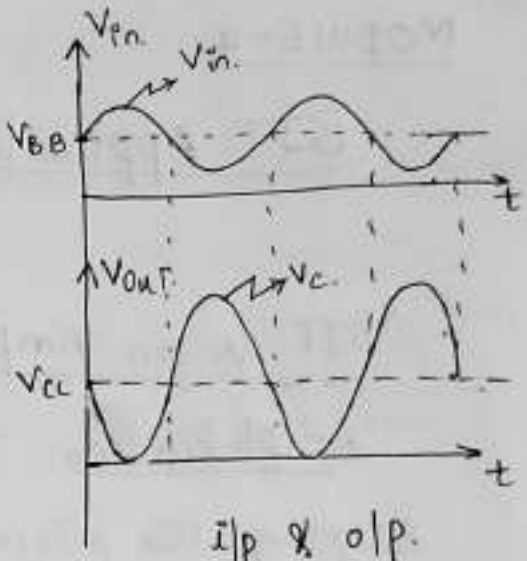
This allows BJTs to be used as amplifiers & switches, giving them wide applicability of it in electronic equipment including computers, televisions, mobile phones, audio amplifiers, industrial control and radio transmissions.

BJTs can be used for both analog and Digital circuits & Both in Ac and DC circuits.

A transistor is a current controlled device. i.e the collector current is equal to the base current multiplied by the current gain β. The base current is very small compared to collector and emitter current

i.e $I_e = I_c + I_b \Rightarrow I_e = I_c \quad [\because I_b \ll I_c]$





i/p & o/p. waveforms.

fig: Basic transistor Amplifier.

Note:

Regions of Operation of Transistor.

J_1 [Emitter-Base]	J_2 [collector-Base]	Region of Operation	Application
1) Forward Bias	Reverse Bias	Active Region.	Amplifier.
2) Forward Bias	Forward Bias	Saturation region	Switch-[ON] [closed ckt]
3) Reverse Bias	Reverse Bias	cutt-off region	Switch-[OFF] [Open ckt]
4) Reverse Bias	Forward Bias	Inverted	Switching Emitter & collector

To operate BJT as an Amplifier it has to be connected in Activeregion. As shown in above figure, the Base emitter junction is forward Biased and collector Base junction

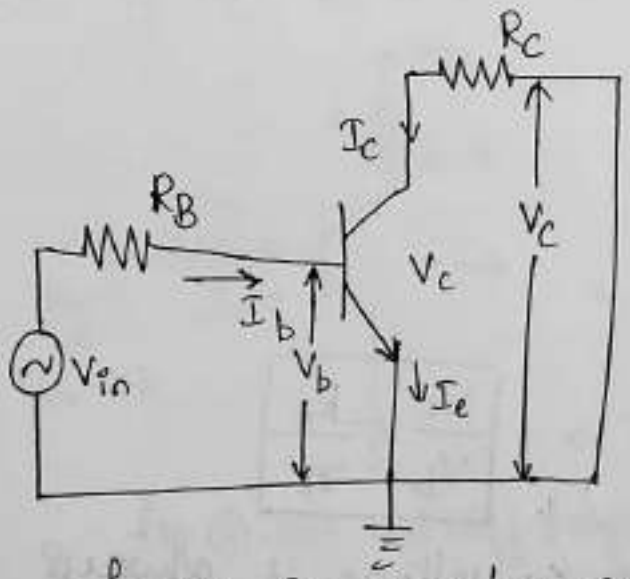
is reverse biased by applying V_{BB} and V_{CC}.

An Ac voltage V_{in} to be amplified is superimposed on the dc bias voltage V_{BB} with the base resistor R_B in series as shown in fig①. The dc bias vlg V_{CC} is connected to the collector through collector resistor R_C.

The ac input voltage V_{in} produces an ac base current which results in a much larger ac voltage across R_C which is amplified and inverted version of ac input voltage as shown in fig①.

[i/p & o/p waveforms].

AC Equivalent circuit



fig②: AC equivalent circuit.

The AC equivalent circuit can be represented by making dc bias sources equal to zero.

i.e $V_{BB}=0$ & $V_{CC}=0$.

The ac equivalent circuit is as shown in fig-②.

The forward biased base emitter junction exhibits a very low resistance to the ac signal V_{in}. This internal ac emitter resistance is designated as r_e'.

From the figure ② the ac emitter current is

$$I_e \simeq I_c = \frac{V_b}{r_e'} \longrightarrow ①$$

The ac collector voltage is,

$$V_c = I_c R_c \simeq I_e R_c \longrightarrow ②$$

By applying KVL to the Base emitter junction we have, $V_b = V_{in} - I_b R_B \longrightarrow ③$.

Let us consider V_b and V_c as transistor ac input and the ac output voltage respectively. The voltage gain i.e the ratio of V_c to V_b is given by,

$$A_v = \frac{V_c}{V_b}$$

from eq ① & eq ②.

$$A_v = \frac{I_e R_c}{I_e r_e'}$$

$$\therefore \boxed{A_v = \frac{R_c}{r_e'}} \Rightarrow \boxed{\frac{V_c}{V_b} = \frac{R_c}{r_e'}}$$

Since $R_c \gg r_e'$, the output voltage is always greater than the input voltage. i.e output voltage V_c is amplified version of V_b.

The current gain is given by, $\boxed{A_i = \frac{I_c}{I_b} = \beta}$

Since $I_C \gg I_b$, A_i is large.

The power gain A_p is defined as the product of the voltage gain A_v and the current gain A_i.

i.e power gain = $\boxed{A_p = A_v \cdot A_i}$

BJT as a SWITCH. [Switching operation of a Transistor]

The Major application of BJT is switch. When BJT is used as an electronic switch, it is operated alternatively in cut-off and saturation regions.

The fig ③-ⓐ & fig ③ ⓑ illustrates the basic operation of BJT as a switching device.

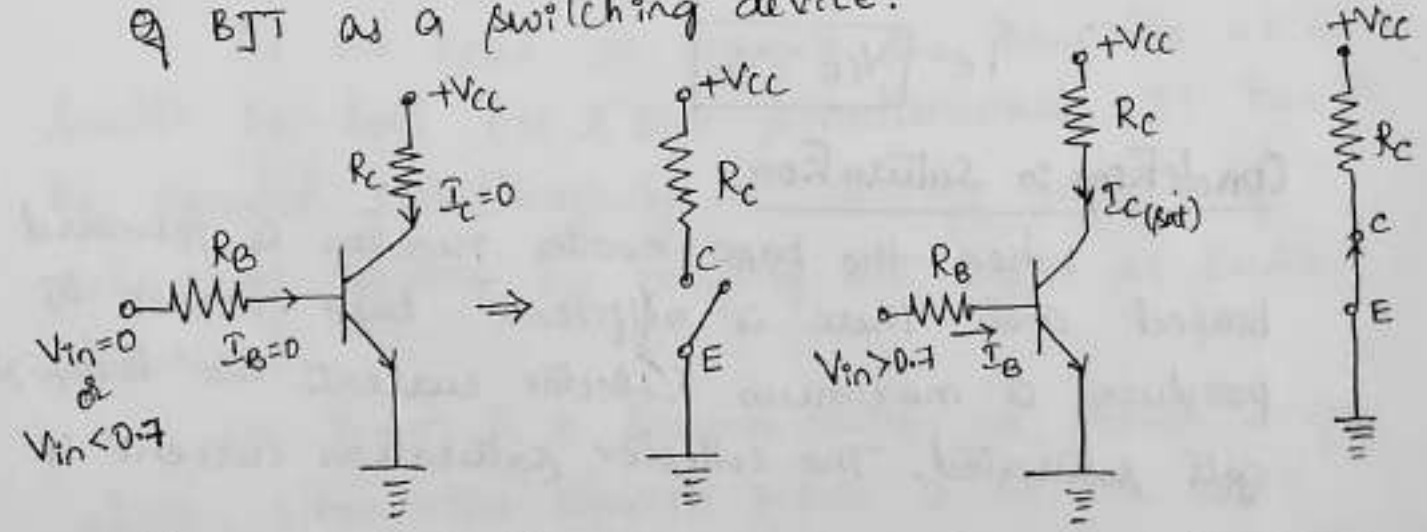


fig ③-ⓐ: cut-off region. [open switch].

fig ③ ⓑ: Saturation region [closed switch].

In fig ③-ⓐ the transistor is in cut off region because the base emitter junction is not forward biased. i.e by applying $V_{in} = 0$ or $V_{in} < 0.7V$.

In cut off region, ideally there is a open between collector and the emitter as shown in fig ③-ⓐ which is represented by open switch.

In fig ③-ⓑ, the transistor is in saturation region, because the base emitter is forward biased and the collector base is forward biased. i.e by applying $V_{in} \geq 0.7$.

In saturation region the transistor is 'Fully-ON'. Maximum collector current flows through the transistor. Transistor operates as a "closed switch". since transistor offers a least resistance as shown in fig. ③-ⓑ.

Conditions in Cutoff: When a transistor is in the cut off region base-emitter junction is not forward biased. Neglecting leakage current, all of the currents are zero. i.e $I_B = 0$ thus $I_C = 0$ and V_{CE} is equal to V_{CC}.

i.e $\boxed{V_{CE} = V_{CC}}$

Conditions in Saturation:

When the base-emitter junction is forward biased and there is sufficient base current to produce a maximum collector current, the transistor gets saturated. The collector saturation current is given by

$$\boxed{I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C}}$$

Since, $V_{CE(sat)}$ is very small compared to V_{CC}. it can be neglected. Hence, the minimum value of base current needed to produce saturation is.

$$I_{B(min)} = \frac{I_{C(sat)}}{\beta_{dc}}$$

Normally. I_B should be considerably greater than $I_{B(min)}$ such that the transistor is saturated.

TRANSISTOR to SWITCH ON/OFF the LED.

The figure ④ shown below is transistor switch to turn ON/OFF an LED.

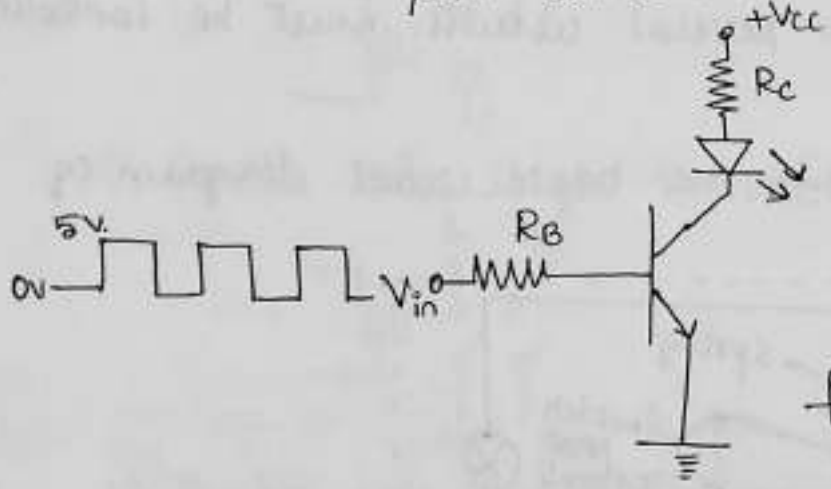


fig ④: Transistor Switch to ON/OFF LED.

As we know to operate the transistor as a switch i.e both ON & OFF simultaneously. It has to be operated simultaneously in cut-off region and saturation region, by varying the input at Base terminal.

Let input is a square wave as shown. In fig above. When the square wave is at 0V, the transistor is in cut-off and there is no collector current. So the LED does not emit light will be in OFF state.

When the square wave goes to high level, the transistor saturates. This forward biases the LED and

the resulting current through the LED caused it to emit light. i.e ON state.

Thus, we have a blinking LED that is ON when V_{in} is high and OFF when $V_{in}=0$.

Note:

Relay: It is an electromagnetic switch. It is used in applications to turn ON and OFF a ckt by a low power signal or when several circuits must be controlled by a one signal.

The below fig shows the basic circuit diagram of Relay.

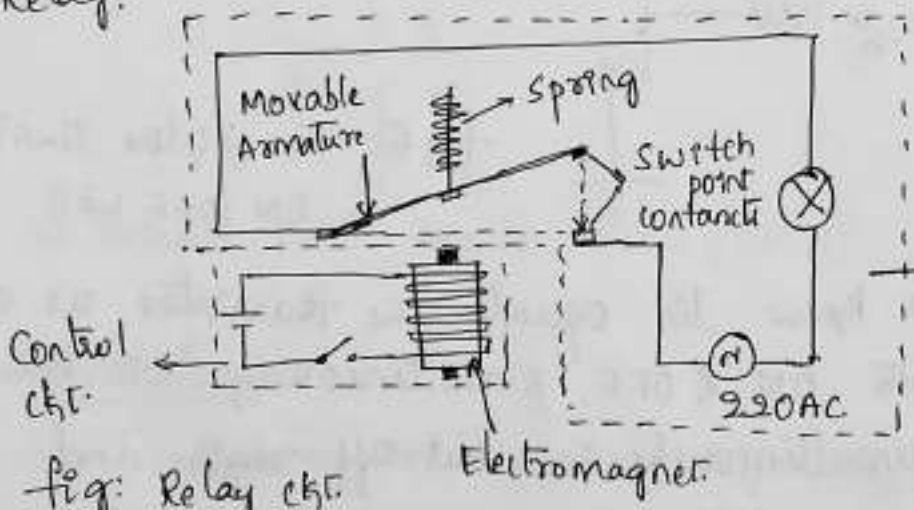


fig: Relay ckt.

The Main parts of Relay: 1) Electromagnet 2) Movable Armature 3) Switch point contacts 4) Spring.

Working: when the control switch is turned 'ON' [closed] current start flowing through a coil. it generates magnetic field that attracts the armature and the load circuit is closed.

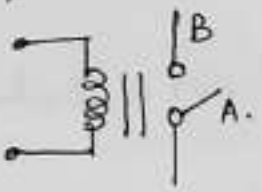
1) This is 'NO' relay [Normally open] - i.e contact is open when relay is not energised.

2) 'NC' Relay - [Normally closed] - i.e contact is closed

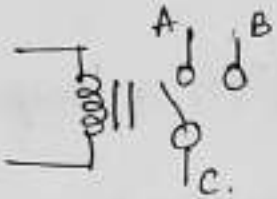
when the relay is not energised.

Types of Relay:

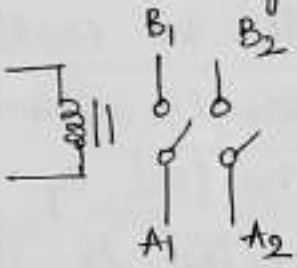
1) Single pole Single throw [SPST].



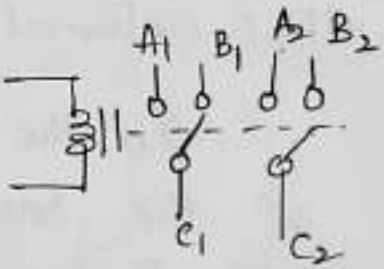
2) Single pole Double throw. [SPDT]



3) Double Pole Single throw [DPST].



4) Double pole Double throw [DPDT].

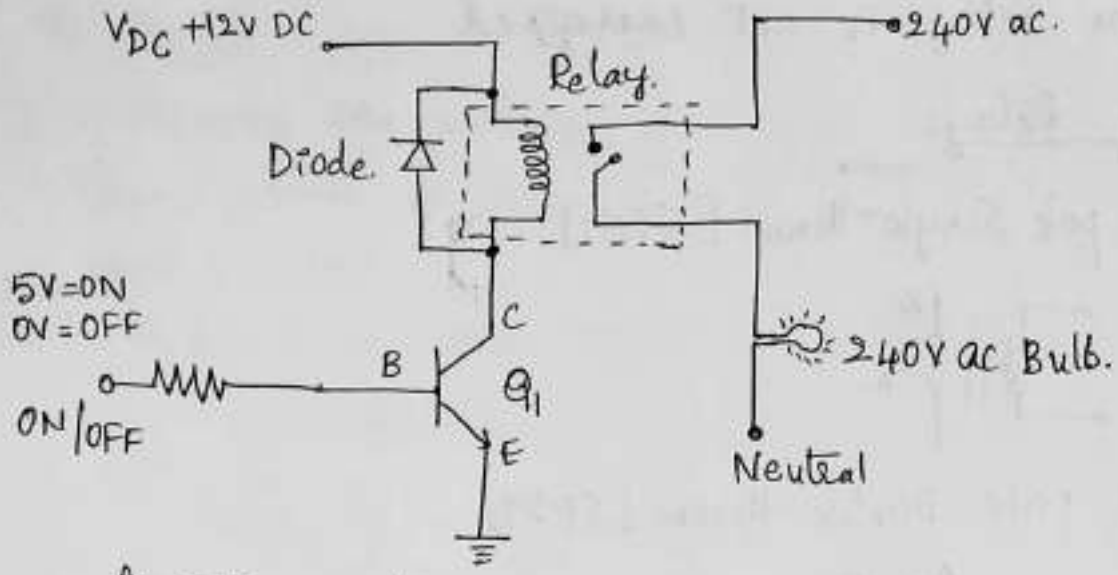


Applications

1) The Railway routing and signaling.
2) Can work like remote, to make a big electronic equipment work
3) Industrial applications, to operate motors and other devices.

TRANSISTOR TO SWITCH ON/OFF a LAMP in a Power Circuit Using a Relay.

The fig-6 shows the transistor to switch ON/OFF a lamp in a power circuit using a relay.



fig⑤: Transistor to switch ON/OFF a lamp in a power circuit using a relay.

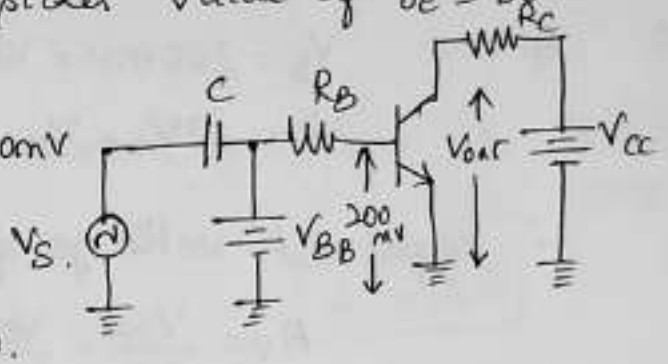
It is also possible to control the relay operation using a transistor as a switch in control circuit of the relay. With a small circuit arrangement of a transistor able to energise the coil of the relay so that external load [bulb] connected to it is controlled.

In the circuit shown above, the input applied at the base causes to drive the transistor into saturation region, which further results the circuit becomes short circuit. So the relay coil gets energised and relay contacts gets operated. which in turn, switch ONs the 240 AC Bulb.

In Inductive loads, sudden removal of power can keep a high potential across the coil. This high voltage can cause considerable damage to the rest of the circuit. Therefore, we have to use the diode in parallel with inductive load to protect the circuit from induced voltages of the inductive load.

Problems:

1) Determine the voltage gain and the AC o/p v/g for the circuit shown in fig. consider value of $r_e' = 50\Omega$ and $R_C = 2K\Omega$.



Soln: Given: $r_e' = 50\Omega$, $V_b = 200mV$

$R_C = 2K\Omega$

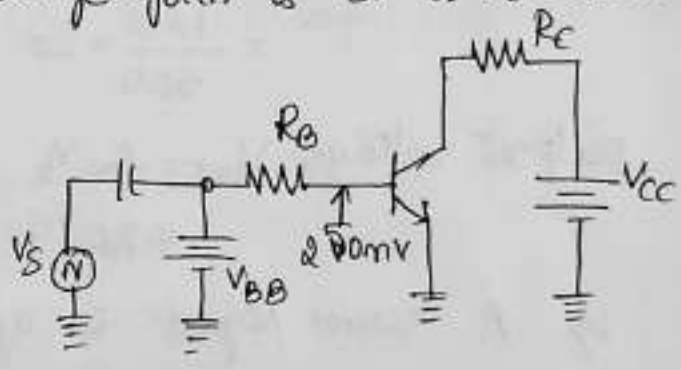
$$A_V = \frac{R_C}{r_e'} = \frac{2K}{50} = 40.$$

The output voltage is given by.

$$V_{out} = A_V \cdot V_b$$
$$= (40) \cdot (200mV).$$

$$\boxed{V_{out} = 8V}$$

2) Determine the value of the R_C for the circuit shown in fig. If the voltage gain is 50 & $r_e' = 50\Omega$.



Soln: Given: $A_V = 50$, $r_e' = 50\Omega$

$V_b = 250mV$

$$A_V = \frac{R_C}{r_e'}$$

$$50 = \frac{R_C}{50\Omega} \Rightarrow \underline{R_C = 2500\Omega \text{ (or) } 2.5K\Omega.}$$

3) A transistor amplifier has a voltage gain of 50. what is the output v/g when the input voltage is 100mV?

Soln: $A_V = 50$

$V_0 = ?$

$V_i = 100mV.$

$$A_V = \frac{V_0}{V_i}$$

$$V_0 = A_V \cdot V_i$$
$$= 50(100) \times 10^{-3} = 5V.$$

④ To acheive an output of 10V with an input of 300mV, what voltage gain is required.

Soln: Given: $V_b = 300mV = V_{in}$

$V_C = 10V. = V_{out}$

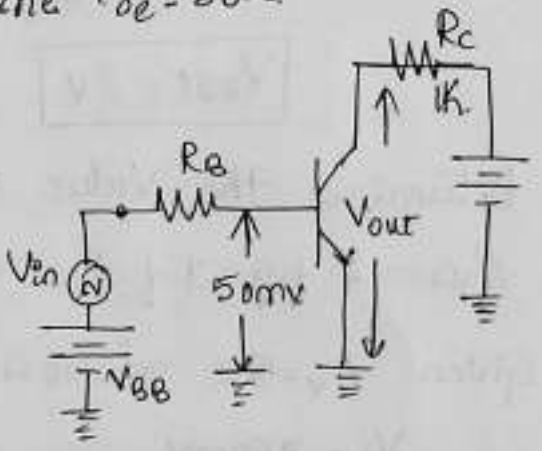
∴ Required voltage gain is

$$A_V = \frac{V_{out}}{V_{in}} = \frac{V_C}{V_b} = \frac{10V}{300mV}$$

$$\boxed{A_V = 33.33}$$

⑤ Determine the voltage gain and the ac o/p voltage for fig shown below. Assume $r_e' = 50\Omega$

Soln:



Voltage gain, $A_v = \frac{R_C}{r_e'}$

$$= \frac{1 \times 10^3}{50\Omega} = 20$$

output voltage, $V_{out} = A_v . V_b$

$$= 20\,(50 \times 10^{-3}) = 1V.$$

6) A 50mV signal is appled to the base of a properly biased transistor with $r_e' = 20\Omega$ and $R_C = 620\Omega$ Determine the output voltage.

Soln: Given: $V_b = 50mV$

$r_e' = 20\Omega$

$R_C = 620\Omega$

Voltage gain, $A_v = \frac{R_C}{r_e'} = \frac{620}{20} = 31$

output voltage, $V_{out} = A_v . V_b$

$= 31\,(50 \times 10^{-3})$

$= 1.55V.$

⇒ A change of 20μA in base current results in a change of 2.5mA in collector current. Calculate the current gain

Soln: Given: $I_b = 20\mu A$, $I_c = 2.5mA$

$\therefore$ current gain $A_i = \frac{I_c}{I_b} = \frac{2.5 \times 10^{-3}}{20 \times 10^{-6}}$

$\boxed{A_i = 125}$

(8) If the voltage gain in certain Amplifier is 110 and the current is 12.5. Calculate the power gain.

Soln: Given: $A_v = 110$, $A_i = 12.5$

$\therefore$ power Gain, $A_p = A_i \times A_v = 110 \times 12.5 = 1375$.

(9) An Amplifier has an input signal of 0.25V and draws 1mA from the source. It delivers 8V to a load at 10mA. Determine the voltage, current and power gains.

Soln: Given $V_b = 0.25V$, $I_b = 1mA$

$V_c = 8V$, $I_c = 10mA$.

Voltage gain, $A_v = \frac{V_{out}}{V_{in}} = \frac{V_c}{V_b} = \frac{8}{0.25} = 32$

current gain, $A_i = \frac{I_c}{I_b} = \frac{10 \times 10^{-3}}{1 \times 10^{-3}} = 10$.

$\therefore$ power gain, $A_p = A_v \cdot A_i = 32 \times 10 = 320$.

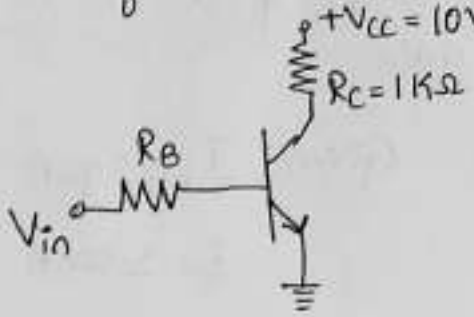
(10) In the circuit shown in fig below,

i) What is V_{CE} when $V_{in} = 0V$?

ii) what minimum value of I_B is required to keep

the BJT in saturation? Given $\beta_{dc} = 200$

iii) Calculate the maximum value of R_B when $V_{in} = 5V$.



Soln: Given: $V_{CC} = 10V$.

$R_C = 1K$.

$\beta_{dc} = 200$.

i) When $V_{in} = 0$, the transistor is in cut-off region.

$\therefore V_{CE} = V_{CC} = 10V$.

ii) Neglecting $V_{CE(sat)}$ i.e $V_{CE(sat)} = 0$.

$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C}$$

$$= \frac{10 - 0}{R_C} = \frac{10}{1 \times 10^3}$$

$$\boxed{I_{C(sat)} = 10\,mA}$$

$$I_{B(min)} = \frac{I_{C(sat)}}{\beta} = \frac{10 \times 10^{-3}}{200} = 50\mu A.$$

This is the minimum value of I_B required to keep the transistor in saturation.

iii) When the input $V_{in} = 5V$.

Voltage across the base resistor R_B, $V_{RB} = V_{in} - V_{BE}$

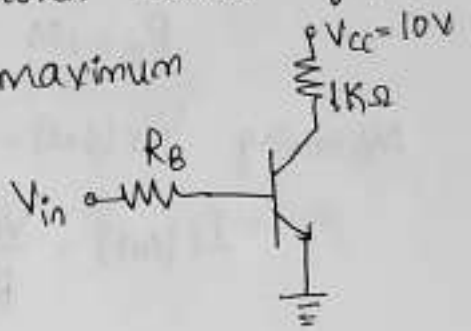
$\therefore V_{RB} = 4.3V$.

$\therefore$ The maximum value of R_B required is

$$R_{B(max)} = \frac{V_{RB}}{I_{B(min)}} = \frac{4.3}{50\mu}$$

$$\boxed{R_{B(max)} = 86K\Omega}$$

11). What is the minimum value of I_B required to saturate the transistor in fig shown below. if $\beta_{dc}=125$ and $V_{CE(sat)} = 0.2V$. Also find the maximum value of R_B required when $V_{in}=8V$.



Soln: Given: $V_{CC}=10V$, $R_C=1K$, $\beta_{dc}=125$.

$V_{CE(sat)} = 0.2V$.

$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C} = \frac{10 - 0.2}{1\times10^3}$$

$$\boxed{I_{C(sat)} = 9.8mA}$$

$$I_{B(min)} = \frac{I_{C(sat)}}{\beta_{dc}} = \frac{9.8\times10^{-3}}{125}$$

$$\boxed{I_{B(min)} = 78.4\mu A}$$

Voltage across, $R_B = V_{RB} = V_{in} - V_{BE} = 8V - 0.7$

$$\boxed{V_{RB} = 7.3V}$$

$$R_{B(max)} = \frac{V_{RB}}{I_{B(min)}} = \frac{7.3}{78.4\times10^{-6}}$$

$$\boxed{R_{B(max)} = 93.11K\Omega}$$

(12) In the circuit shown in fig below,

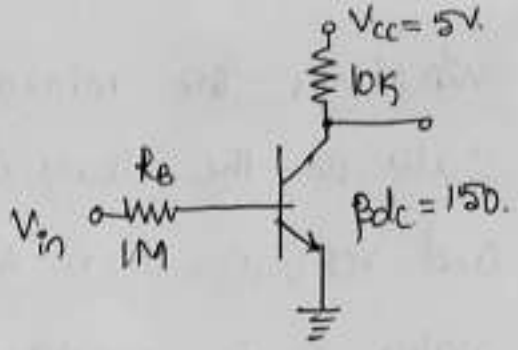
i) what is the value of I_B necessary to produce saturation.

ii) what minimum value of V_{in} is necessary for saturation? Assume $V_{CE(sat)} = 0V$.

Soln: Given: $V_{CC} = 5V$ $R_C = 10K$

$\beta_{dc} = 150$

$R_B = 1M$



Assuming $V_{CE(sat)} = 0V$.

$$I_{C(sat)} = \frac{V_{CC}}{R_C} = \frac{5}{10K} = 500\,\mu A. = 0.5mA.$$

i) ∴ minimum I_B required.

$$I_{B(min)} = \frac{I_{C(sat)}}{\beta_{dc}} = \frac{500\mu A}{150} = 3.33\,\mu A.$$

ii) $$I_B = \frac{V_{in} - V_{BE}}{R_B}$$

$I_{B(min)}$ when V_{in} is minimum.

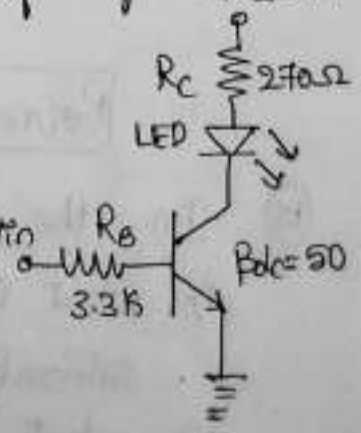
$$\therefore I_{B(min)} = \frac{V_{in(min)} - V_{BE}}{R_B}$$

$$V_{in(min)} = I_{B(min)} R_B + V_{BE}$$

$$= (3.33\mu)(1M) + 0.7$$

$$\boxed{V_{in(min)} = 4.03V}$$

(13) The LED used in fig as shown below requires 30mA to emit a sufficient level of light. Determine the amplitude of the square wave input voltage necessary to make sure that the transistor saturates. Use double the $I_{B(min)}$ to ensure saturation Assume $V_{CE(sat)} = 0.3V$.



V_{in} =

Soln: $I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C} = \frac{9-0.3}{270} = 32.2mA (> 30mA)$

$\therefore I_{B(min)} = \frac{I_{C(sat)}}{\beta dc} = \frac{32.2m}{50} = 644\mu A.$

To ensure saturation use double the value of $I_{B(min)}$.

$\therefore I_B = 2 \times 644\,\mu A = 1288\mu A.$

$I_B = \frac{V_{in} - V_{BE}}{R_B}$

$I_{B(min)} = \frac{V_{in(Min)} - V_{BE}}{R_B}$

$V_{in(min)} = I_B R_B + V_{BE}$

$= 1288\mu (3.3K) + 0.7 = 4.96V.$

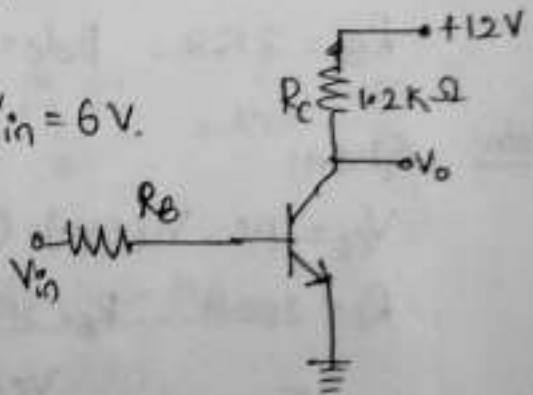
$\therefore$ the amplitude of the square wave input v/g must be atleast 4.96V.

(14) For the ckt shown in fig. below. $V_{in} = 0V$.

a) Find the value of V_{CE} when $V_{in} = 0V$.

b) If $\beta dc = 220$ with negligible $V_{CE(sat)}$. Determine the minimum value I_B required to saturate the transistor

c) Find the $R_{B(max)}$ when $V_{in} = 6V$.



Soln: Given $R_C = 1.2K\Omega$.

$V_{CC} = 12V$

a) when $V_{in} = 0$, $V_{CE} = V_{CC} = 12V$.

b) $\beta dc = 220$, $V_{CE(sat)} = 0$

$$\therefore I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C} = \frac{12 - 0}{1.2K} = 10mA.$$

$$I_{B(min)} = \frac{I_{C(sat)}}{\beta_{dc}} = \frac{10 \times 10^{-3}}{220} = 45.45\mu A.$$

c) Let us consider $V_{BE} = 0.7V$, we have $V_{in} = 6V$. On applying KVL to the i/p side.

$$V_{in} - V_{RB} - V_{BE} = 0$$

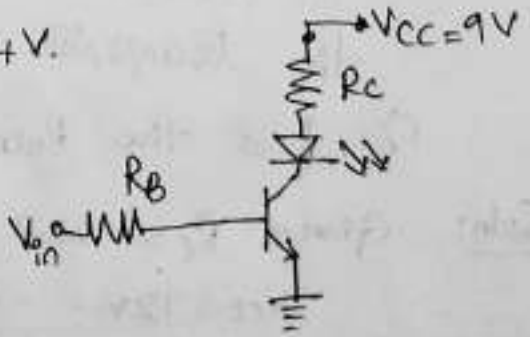
$$V_{RB} = 6 - 0.7 = 5.3V.$$

$$R_{B(max)} = \frac{V_{in(min)} - V_{BE}}{I_{B(min)}}$$

$$= \frac{6 - 0.7}{45.45 \times 10^{-6}}$$

$$\boxed{R_B = 116K\Omega}$$

15). For the circuit shown in fig below. LED requires 34mA to emit Light. Determine the value of i/p voltage required to saturated transistor. TO ensure saturation use twice the value of $I_{B(min)}$. Consider $V_{CC} = 9V$, $V_{CE(sat)} = 0.4V$, $R_C = 200\Omega$ $R_B = 3K\Omega$, $\beta_{dc} = 45$, $V_{LED} = 1.4V$.



Soln: Given:

$V_{CC} = 9V$, $V_{CE(sat)} = 0.4V$

$R_C = 200\Omega$, $R_B = 3K\Omega$

$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)} - V_{LED}}{R_C} = \frac{9 - 0.4 - 1.4}{200}$$

$$I_{C(sat)} = 36mA.$$

$$I_{B(min)} = \frac{I_{C(sat)}}{\beta_{dc}} = \frac{36 \times 10^{-3}}{45} = 800\mu A.$$

To saturate transistor consider twice the value of $I_{B(min)}$; i.e $I_B = 2 I_{B(min)} = 2 \times 800\,\mu A.$

$= 1.6\,mA$

$$V_{in} = I_B R_B + V_{BE}$$

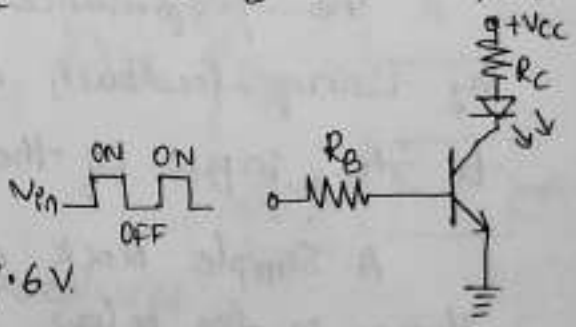
$$= 1.6 \times 10^{-3} \times 3 \times 10^{3} + 0.7.$$

$$= 4.8 + 0.7.$$

$$\boxed{V_{in} = 5.5V}$$

(16) In the circuit shown in fig below, LED requires 30mA to emit a sufficient level of light. Therefore the collector current should be approximately 30mA. For the following circuit values determine the amplitude of the square wave input voltage necessary to make sure that the transistor saturates. Use double the minimum value of base current as a safety margin to ensure saturation.

$V_{CC} = 9V$, $V_{CE(sat)} = 0.3V$, $R_C = 220\Omega$, $R_B = 3.3K\Omega$, $\beta_{dc} = 50$ and $V_{LED} = 1.6V$.



Soln: Given: $V_{CC} = 9V$, $R_C = 220\Omega$, $R_B = 3.3K$, $\beta_{dc} = 50$, $V_{LED} = 1.6V$

$$I_{C(sat)} = \frac{V_{CC} - V_{LED} - V_{CE(sat)}}{R_C} = \frac{9 - 1.6 - 0.3}{220}$$

$$\boxed{I_{C(sat)} = 32.3mA}$$

$$I_{B(min)} = \frac{I_{C(sat)}}{\beta_{dc}} = \frac{32.3 \times 10^{-3}}{50} = 646\mu A.$$

To ensure saturation, use twice the value of $I_{B(min)}$ which is 1.29 mA

$$I_B = \frac{V_{RB}}{R_B} = \frac{V_{in} - V_{BE}}{R_B}$$

$$V_{in} = I_B R_B + V_{BE}$$
$$= (1.29 \times 10^{-3})(3.3 \times 10^{3}) + 0.7$$

$$\boxed{V_{in} = 4.96V}$$

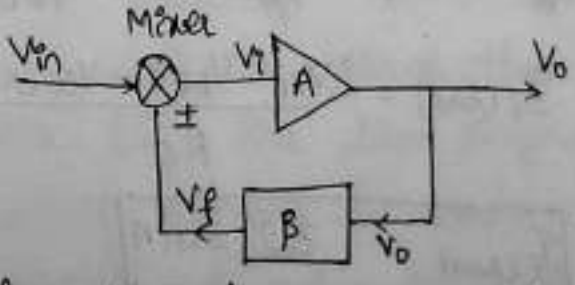
FEEDBACK AMPLIFIERS

Feedback Amplifiers are the Amplifiers in which some portion of the output is fedback to the input along with the source input.

The purpose of the Amplifier is to amplify the input signal without changing any of its any characteristics except the amplitude.

The performance of an amplifier can be improved by using feedback ckt which connects the output to the input of the amplifier.

A Simple block diagram a feedback amplifier is shown in fig below.



V_{in} → source i/p
V_i → i/p to Amplifier
V_o → output
V_f → feedback signal.

fig: Block diagram of feedback Amplifier

The input signal V_{in} is applied to a mixer network in which it is combined with feed signal V_f. The difference of these signals is the V_i, I/p to the amplifier. A portion of the amplifier o/p is connected to the I/p side through a feedback n/w (β).

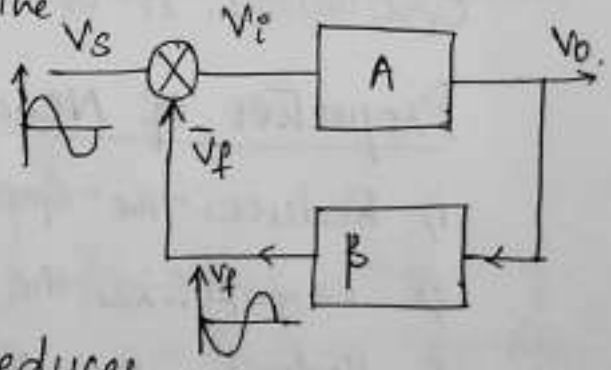
The feedback is very important because, it can allow us to change certain important characteristics of the amplifier in a desired manner.

There are two types Feedback connections.

1) Positive Feedback
2) Negative Feedback.

Negative Feedback: If the feedback signal is in opposite phase w.r.t the source input then it is called as Negative feedback.

In the negative feedback, the feedback signal will be subtracted from the source signal. i.e $\boxed{V_i = V_s - V_f}$

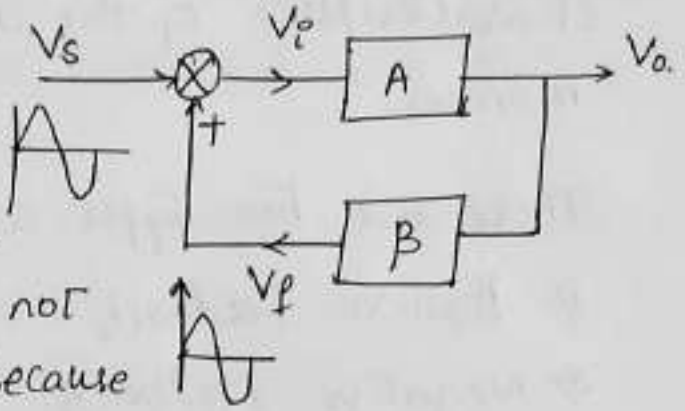


The Negative feedback reduces the overall gain of the amplifier since the i/p signal is the difference b/w the two signals. Although negative feedback results in reduced overall gain. A number of properties & advantages can be

obtained from Negative feedback. Negative feedback is the most commonly used feedback connection in Amplifiers. It is also called inverse feedback & degenerative feedback.

Positive feedback: It is the type of feedback connection in which feedback signal is added along with source input. & If the feedback signal is in phase with input source signal then it is called positive feedback.

i.e $V_i = V_s + V_f$



Though positive feedback increases the overall gain of the amplifier. It is not used in the amplifiers, because +ve feedback causes distortion and instability in amplifiers.

+ve feedback amplifiers increases the gain & overall power of the o/p signal and hence used in Oscillators. It is also called direct feedback & Regenerative feedback.

Properties of Negative Feedback

1) Reduces the Gain
2) Desensitizes the Gain
3) Reduces the Non-linear distortion
4) Reduces the effect of Noise
5) Controls the input and output resistance.
6) Extended Bandwidth of the Amplifier.

Advantages of Negative feedback

Although negative feedback results in reduced gain, it has many advantages.

1) Low output resistance of a voltage amplifier can be further lowered
2) High input resistance of a voltage amplifier can be increased
3) There is a improvement in linearity of operation of the feedback amplifier compared with that of the amplifier without feedback
4) The transfer gain Af of amplifier with feedback can be stabilized against variation of h & hybrid π parameters of the transistors
5) Use of negative feedback improves frequency response of the amplifier i.e increases the Bandwidth.

Principle of Negative feedback Amplifier

Consider a block diagram of a negative feedback amplifier shown in fig.

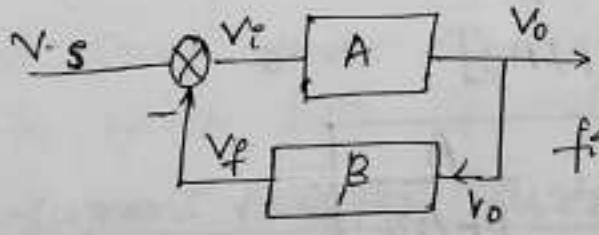


fig: Block diagram of -ve feedback Amplifier.

Where, V_s = Source input
V_i = input to the Amplifier
β = Gain of the feedback nlw
A = Gain of the basic amplifier
V_o = o/p of the Amplifier.

The Gain of the basic amplifier & open loop gain of the amplifier is, $A = \frac{V_o}{V_i}$ → ①

The overall gain of the amplifier & closed loop gain of the amplifier is, $A_f = \frac{V_o}{V_s}$ → ②

from ① $V_o = A \cdot V_i$ → ③.

we have, $V_i = V_s - V_f$. → ④.

For the feedback n/w.

$$\beta = \frac{V_f}{V_o} \rightarrow ⑤$$

$$\Rightarrow V_f = \beta \cdot V_o. \rightarrow ⑥$$

Substituting eq-④ in ③

$$V_o = A[V_s - V_f]$$

$$V_o = A \cdot V_s - AV_f.$$

from eq-⑥

$$V_o = A \cdot V_s - A \cdot \beta V_o.$$

$$V_o + A\beta V_o = A \cdot V_s$$

$$V_o[1 + A\beta] = A \cdot V_s$$

$$\boxed{\frac{V_o}{V_s} = \frac{A}{1 + A\beta}}$$

∴ The overall gain of the amplifier with feedback is

$$\boxed{A_f = \frac{V_o}{V_s} = \frac{A}{1 + A\beta}} \rightarrow ⑦$$

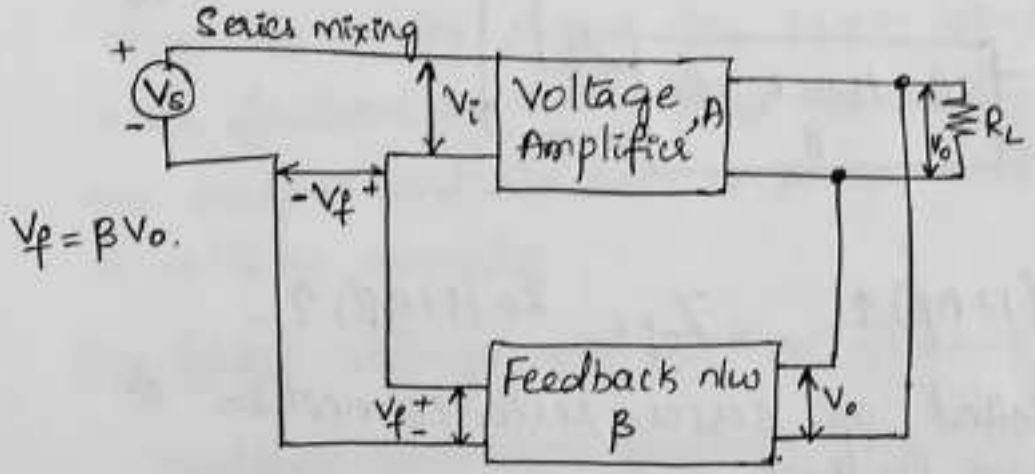
The Negative feedback reduces the gain by a factor $(1+A\beta)$.

Types of Negative Feedback.

There are 4 types of negative feedback topologies Both voltage and current can be feedback to the i/p either in series & parallel. They are.

1) Voltage - series feedback
2) Voltage - shunt feedback
3) current series feedback
4) current shunt feedback.

1) Voltage Series feedback Amplifier



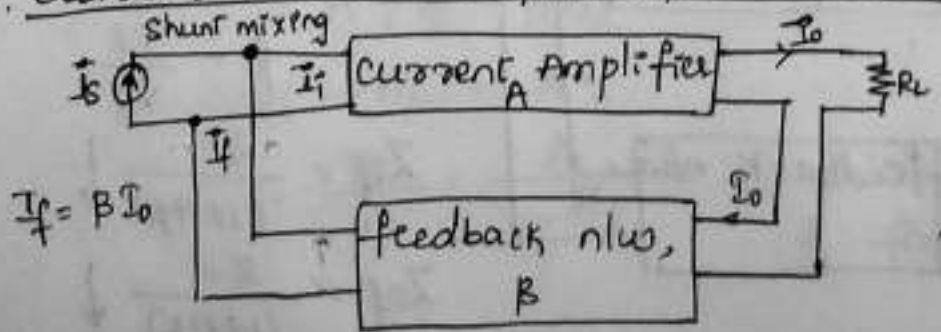
$A = \frac{V_o}{V_i}$

$\beta = \frac{V_f}{V_o}$.

$\uparrow Z_{if} = Z_i(1+A\beta)$ $\quad Z_{of} = \frac{Z_o}{(1+A\beta)} \downarrow$

Also called Series - shunt connection & voltage-voltage Amplifier in which both i/p and o/p are voltages.

2). Current - current Amplifier / current shunt feedback



$A = \frac{I_o}{I_i}$

$\beta = \frac{I_f}{I_o}$.

It is also called voltage shunt feedback & shunt-shunt connection.

Voltage Series Feedback Amplifier.

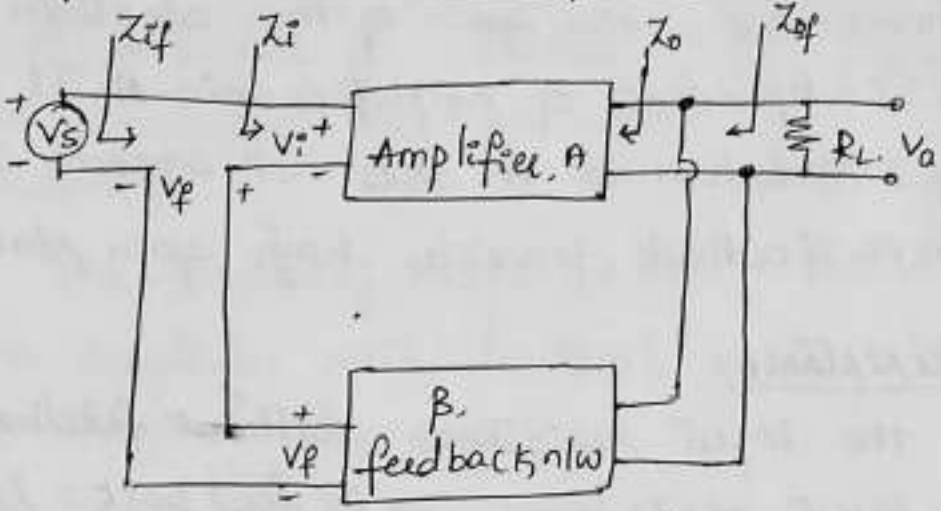


fig: Block diagram of voltage series feedback Amplifier

The above fig shows the block diagram of voltage series feedback amplifier. Here the voltage is sampled at the output and fed back in series with input. It is a voltage amplifier.

i) **Gain:** Voltage gain without feedback, $A = \frac{V_o}{V_i}$

Voltage gain with feedback, $A_f = \frac{V_o}{V_s}$

Feedback factor, $\beta = \frac{V_f}{V_o}$

$$V_o = A \cdot V_i$$
$$= A (V_s - V_f)$$
$$= A (V_s - \beta V_o)$$
$$V_o (1 + A\beta) = A V_s$$
$$\therefore \frac{V_o}{V_s} = \frac{A}{1 + A\beta} = A_f \Rightarrow \text{voltage gain with feedback.}$$

The voltage gain of the amplifier with feedback reduces by a factor of $(1+A\beta)$.

if $A\beta > 1$ then $A_f = \frac{1}{\beta}$

It shows that, the gain of the amplifier with feedback is independent of amplifier gain A. It means that any variation in A does not appear in A_f i.e negative feedback provides high gain stability.

ii) Input Resistance:

Let the input resistance without feedback $= Z_i$ and the input resistance with feed back $= Z_{if}$

In voltage series feedback amplifier, the output of the feedback nlw is connected in series with the i/p of amplifier. Therefore Z_{if} is greater than Z_i.

$$\boxed{Z_{if} = Z_i(1+A\beta)}$$

iii) Output Resistance:

Let the output resistance of Amplifier without feedback $= Z_o$ and

the output resistance of Amplifier with feedback $= Z_{of}$

In voltage series feedback amplifier the i/p of the feedback nlw is connected in parallel to the o/p of the amplifier. As a result Z_{of} is smaller than Z_o and is given by $\boxed{Z_{of} = \frac{Z_o}{1+A\beta}}$

iv) Gain & Bandwidth

Negative feedback reduces the overall gain of the Amplifier. But the gain-Bandwidth product of an amplifier is constant the Bandwidth increases with feedback.

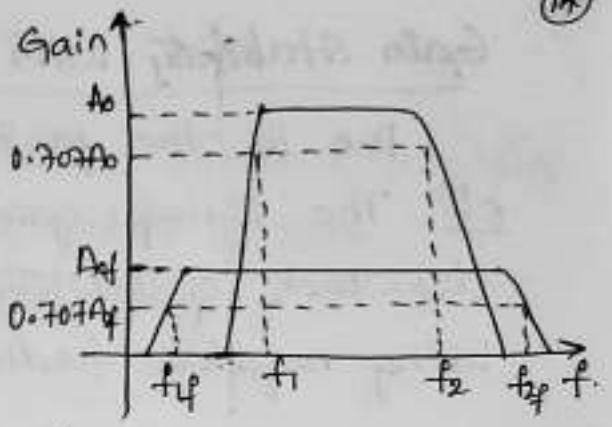


fig: Effect of negative feedback on Gain & B.W.

The frequency response of the amplifier with feedback and without feedback is as shown in fig. above.

Bandwidth without feedback, $B.W = f_2 - f_1 \simeq f_2 \; [\because f_2 \gg f_1]$

Bandwidth with feedback, $B.W_f = f_{2f} - f_{1f} \simeq f_{2f} \; [\because f_{2f} \gg f_{1f}]$

A_o is the midband gain without feedback

A_{of} is the midband gain with feedback.

At higher frequency, amplifier acts as low pass filter

Gain of the amplifier without feedback,

$$A = \frac{A_o}{1 + \left(j\frac{w}{w_2}\right)}$$

Gain of the amplifier with feedback

$$A_f = \frac{A_{of}}{1 + j\left(\frac{w}{w_{2f}}\right)}$$

The Gain Bandwidth product is constant for with feedback and with out feedback

$$\therefore \boxed{A_o f_2 \simeq A_{of} f_{2f}}$$

Gain Stability with Feedback

Due to the factors like operating point, temperature etc. The transfer gain of amplifier is not constant. This drawback of stability in amplifier can be decreased using negative feedback.

$$A_f = \frac{A}{1+A\beta}$$ } overall gain of the Amplifier with feedback.

differentiating on both sides w.r.t A.

$$\frac{dA_f}{dA} = \frac{(1+A\beta)1 - \beta A}{(1+A\beta)^2} = \frac{1}{(1+A\beta)^2}$$

$$\frac{dA_f}{dA} = \frac{A_f}{A(1+A\beta)} \quad \left[\because \frac{A_f}{A} = (1+A\beta)\right]$$

$$\boxed{\frac{dA_f}{A_f} = \frac{1}{(1+A\beta)}\left[\frac{dA}{A}\right]}$$

If $A\beta \gg 1$ $\quad \frac{dA_f}{A_f} = \frac{1}{\beta A}\left[\frac{dA}{A}\right]$

The above equation represents relative change $\frac{dA_f}{A_f}$ in the overall gain of the amplifier is reduced by a factor βA in the relative change $\frac{dA}{A}$ in the basic amplifier

where,

$\frac{dA_f}{A_f}$ = fractional change in amplification with feedback

$\frac{dA}{A}$ = fractional change in amplification without feedback.

Problems:

1) Calculate the gain of the negative feedback amplifier having $A=2000$. If the feedback factor is 20%.

Soln: Given: $A=2000$, $\beta = 20\% = 0.2$, $A_f = ?$

$$A_f = \frac{A}{1+A\beta}$$

$$= \frac{2000}{1+(2000)(0.2)} = 4.98$$

2) An Amplifier without feedback has voltage gain of 2000. If the voltage gain changes by 20% due to variation in temperature, find the change in gain of the feedback amplifier. Given that $\beta = 0.1$

Soln: Given: $A=2000$, $\beta = 0.1$. $\% \frac{dA}{A} = 20\% = 0.2$.

we have,

$$\frac{dA_f}{A_f} = \frac{1}{A\beta+1}\left[\frac{dA}{A}\right]$$

$$= \frac{1}{1+(2000)(0.1)}[0.2]$$

$$\frac{dA_f}{A_f} = 0.000995$$

$$\% \frac{dA_f}{A_f} = 0.0995\%$$

3) An Amplifier has a bandwidth of 200KHz and voltage gain of 1000

i) what will be the new bandwidth and the gain if 5% of negative feedback is employed.

ii) what is the gain bandwidth product with and without

feedback.

iii) What must be the feedback factor required for the bandwidth to be 1MHz.

Soln: Given: $A = 1000$. $B.W = 200KHz$.

i) $\beta = 5 - 1 = 0.05$

$$A_f = \frac{A}{1+A\beta} = \frac{1000}{1+(1000)(0.05)} = \frac{1000}{51}$$

$$A_f = 19.6$$

Bandwidth with feedback: $(B.W)_f = B.W(1+A\beta)$

$= 200K[1+50]$

$= 10.2MHz.$

or

$$(B.W)_f \cdot A_f = (B.W) \cdot A.$$

$$(B.W)_f = \frac{[B.W] \times A}{A_f} = 10.2MHz.$$

ii) Gain Bandwidth product.

with feedback $= [B.W]_f \cdot A_f = (10.2 \times 10^6)(19.6)$

$= 199.9 \simeq 200MHz$

without feedback $= [B.W] \cdot A = [200][1000] = 200MHz.$

iii) Given: $(B.W)_f = 1MHz.$

$$(B.W)_f = (1+A\beta) B.W.$$

$$1 \times 10^6 = [1 + 1000\beta][200 \times 10^3].$$

$$\beta = 0.004 = 0.4\%$$

4) A feedback amplifier consists of 2 amplifiers connected in series each having voltage gain of 100

i) what should be the feedback factor to have an

overall gain of 100?

ii) If the gain of each amplifier reduces to 50 due to parameter variations, what is the change in the overall gain?

Soln: i) Two amplifiers are connected in series.

∴ Gain without feedback $A = 100 \times 100 = 10^4$.

The overall gain required = Gain with feedback = $A_f = 100$.

$$\therefore A_f = \frac{A}{1 + A\beta}$$

$$100 = \frac{10^4}{1 + 10^4 \cdot \beta}$$

$$\therefore \boxed{\beta = 0.0099} \Rightarrow \% \beta = 0.99\%$$

ii) The gain of each amplifier reduces to 50.

∴ Gain without feedback : $A = 50 \times 50 = 2500$

∴ New overall gain,

$$A_f = \frac{A}{1 + A\beta}$$

$$= \frac{2500}{1 + (2500)(0.0099)}$$

$$\boxed{A_f = 97.09}$$

∴ Change in the overall gain = 100 - 97.09

= 2.91 or 2.91%

5) Given that gain without feedback $A = 10^5$ and with feedback $A_f = 50$ and $\beta = 0.01999$. If the change in the gain without feedback is 10^4, find the percentage change in gain with feedback.

Soln: Given: $A = 10^5$, $A_f = 50$ and $\beta = 0.01999$

Change in gain without feedback $dA = 10^4$.

$\therefore$ % change in gain without feedback $= \frac{dA}{A} \times 100$

$= \frac{10^4}{10^5} \times 10^2$

$= 10\% = 0.1$.

$$\frac{dA_f}{A_f} = \frac{1}{1+A\beta}\left[\frac{dA}{A}\right].$$

$$\frac{dA_f}{A_f} = \frac{1}{1+(10^5)(0.01999)}[0.1].$$

$$\frac{dA_f}{A_f} = 5 \times 10^{-5}$$

$$\%\ \frac{dA_f}{A_f} = 5 \times 10^{-5} \times 100 = 0.0005\%$$

6). The gain factors in a feedback ckt are $A = 5 \times 10^5$ and $A_f = 100$. The parameter A_f must not change more than $\pm 0.001\%$ due to change in A. What is the maximum allowable variation in A.

Soln: Given: $A = 5 \times 10^5$, $A_f = 100$, $\%\ \frac{dA_f}{A_f} = 0.001\%$

$$A_f = \frac{A}{1+A\beta}$$

$$100 = \frac{5 \times 10^5}{1+(5 \times 10^5)\beta}$$

$$\beta = 0.009998 \qquad \%\ \beta = 0.9998\%$$

$$\frac{dA_f}{A_f} = \frac{1}{1+A\beta}\left[\frac{dA}{A}\right]$$

$$0.001 = \frac{1}{1+(0.009998)(10^5 \times 5)}\left[\frac{dA}{A}\right]$$

$$\Rightarrow \frac{dA}{A} = 5\%$$

∴ Allowable % change in A is ±5%

7. An Amplifier with open loop gain $A = 1000 \pm 150$ is available. There is a necessity of an amplifier whose voltage gain varies by no more than ±0.15 %.

find i) β of the feedback now used

ii) Gain with feedback.

Soln: Given: $A = 1000 \pm 150$, $\frac{dAf}{Af} = 0.15\%$, $\frac{dA}{A} = \frac{\pm 150}{1000} = 0.15$

i) $\frac{dAf}{Af} = \frac{1}{1+\beta A}\left[\frac{dA}{A}\right]$. % $\frac{dA}{A} = 15\%$

$$[0.15\%] = \frac{1}{1+A\beta}[15\%]$$

$$\therefore 1+A\beta = 100$$

$$\boxed{\beta = 9.9\%}$$

ii) The Gain with feedback is given by,

$$A_f = \frac{A}{1+A\beta}$$

$$= \frac{1000}{1+(0.099)(1000)}$$

$$\boxed{A_f = 10}$$

⑧ An Amplifier has a high frequency response described as $A = \frac{A_0}{1+j(\omega/\omega_2)}$. Where in $A = 1000$, $\omega_2 = 10^4$ rad/s. Find the feedback (negative) factor β. which will raise the upper corner frequency (ω_2) to 10^5 rad/s. What is the corresponding overall gain of the amplifier? Find also the gain-bandwidth product in each case.

Soln: Given, $A = 1000$, $\omega_2 = 10^4$ rad/s, $\omega_{2f} = 10^5$ rad/s.

from Gain Bandwidth product.

$$A.(B.W) = A_f.(B.W)_{2f}.$$

$$A.\omega_2 = A_f.\omega_{2f}.$$

$$A_f = \frac{A.\omega_{2f}}{\omega_2} = \frac{1000 \times 10^5}{10^4}$$

$$\boxed{A_f = 100.}$$

Gain Bandwidth product without feedback $= A.(B.W)$

$= 1000 \times 10^4$

$= 10^7$

Gain Bandwidth product with feedback $= A_f.(B.W)_f$

$= 100 \times 10^5$

$= 10^7.$

OSCILLATORS.

Oscillators are defined as an electronic circuit which essentially produces a signal output waveform even without input signal excitation.

(or) Oscillator is an electronic circuit which converts d.c/g to a.c oscillations.

Applications:

1) To generate sinusoidal signals which are used in radio and TV broad cable.

2) To generate square wave which are used as a clock signals in computation, mobile phones and other digital systems.

3) In Signal generators, which are used in laboratories to test the ckts.

4) In the communication system to generate the Carrier signals.

Classification of oscillators:

Oscillators can be classified based on various criteria

a) Based on operating principle

i) Feedback oscillators

ii) Negative resistance effect oscillators.

b) Based on type of output waveforms

i) Sinusoidal oscillators or harmonic oscillators.

ii) Non-sinusoidal oscillators or Relaxation oscillators

c) Based on Feedback ckt employed

i) Rc oscillators ii) Lc oscillators.

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i) Rc oscillators ii) Lc oscillators.

d) Based on frequency of the generated signals.

i) Audio frequency (AF) oscillators (A few Hz to 20KHz).

ii) Radio frequency (RF) oscillators (20KHz to 30MHz).

iii) Very High frequency (VHF) oscillators [30MHz - 300MHz]

iv) Ultra High frequency (UHF) oscillators [300MHz - 3GHz].

v) Microwave oscillators.

Concept of Feedback:

Feedback is used to improve the performance of a device and to make it more ideal.

Positive feedback is used in case of oscillators i.e the feed signal is in phase in the source input signal. Positive feedback results into oscillations and hence used in electronic circuits.

Consider the oscillator ckt. shown in fig. with Amplifier gain 'A' & feedback factor β.

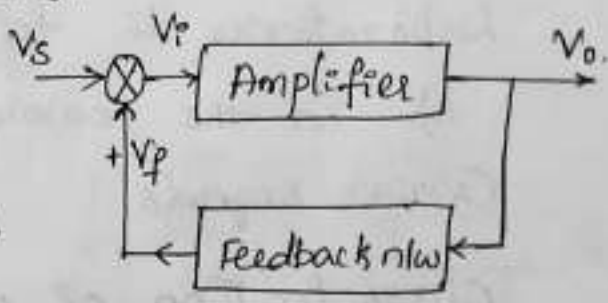


fig: Concept of feedback

Then $A = \frac{V_o}{V_i}$ → loop gain of the amplifier.

The closed loop gain of the circuit & gain with feedback is given by, A_f.

$$A_f = \frac{V_o}{V_s}$$

V_f is added to the input of the amplifier.

$$\therefore V_i = V_s + V_f$$

and from $\beta = \frac{V_f}{V_o} \Rightarrow V_f = \beta V_o$.

$$\therefore V_i = V_s + \beta V_o.$$

$$V_s = V_i - \beta V_o.$$

$$A_f = \frac{V_o}{V_s} = \frac{V_o}{V_i - \beta V_o.}$$

Dividing the numerator & Denominator by V_i. in the above equation.

$$A_f = \frac{V_o/V_i}{V_i/V_i - \beta V_o/V_i}$$

$$\boxed{A_f = \frac{A}{1 - A\beta}}$$

The above equation shows that gain with feedback increases as the amount of positive feedback increases.

Barkhausen Criterion

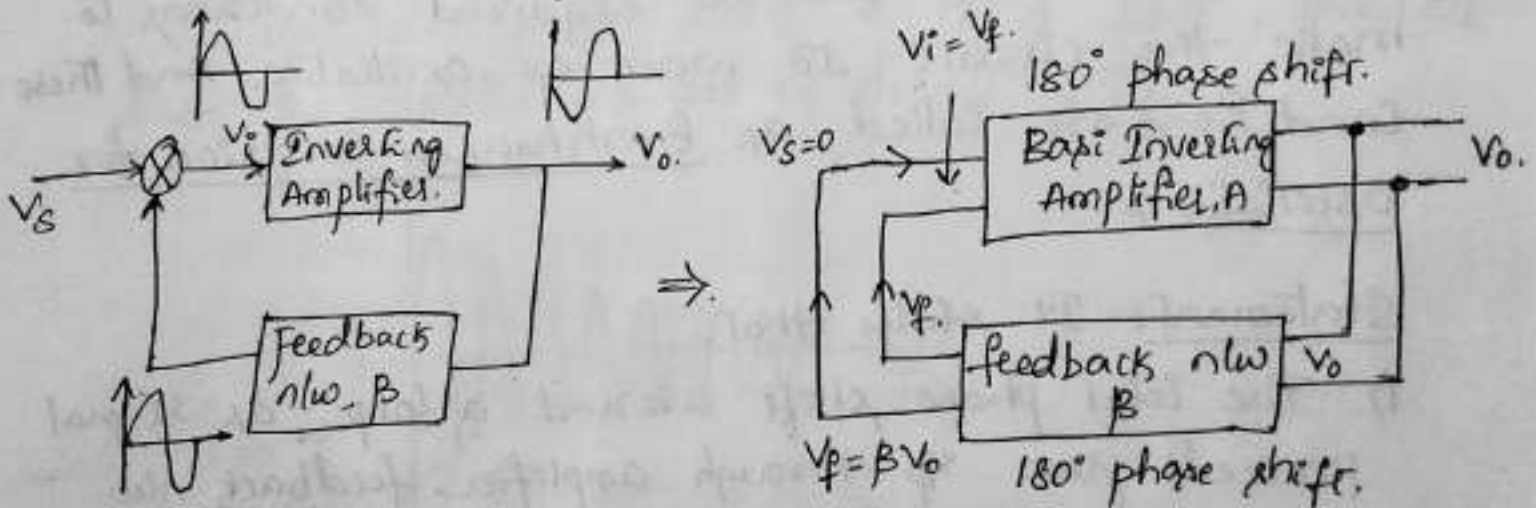


fig: Amplifier with +ve feedback.

Consider a Basic Inverting Amplifier with a Open loop gain A, feedback nlw attenuation factor or feedback factor $\beta < 1$ as shown in figure above.

The Basic amplifier is inverting it produces phase shift of 180° blw i/p & o/p. as the feedback

must be positive. o/p of the feedback n/w must be in phase with V_s. Hence n/w uses a phase shift of 180° while feeding back v/g from o/p to i/p. this ensures +ve feedback.

From the above figure.

$$V_o = AV_i \longrightarrow (1)$$

$$V_f = \beta \cdot V_o \longrightarrow (2)$$

Substitute eq (1) in (2).

$$V_f = \beta \cdot AV_i.$$

$$\boxed{V_f = A\beta \cdot V_i}$$

when $|A\beta| = 1$ then $\boxed{V_f = V_i} \Rightarrow V_s = 0$.

and total phase shift around loop is 360°.

The above two are the required conditions to make the circuit to work as oscillator. And these conditions are called as Barkhausen Criterion for Oscillations.

Statement: It states that.

1) The total phase shift around a loop, as signal proceeds from i/p through amplifier, feedback n/w back n/w to i/p again completing a loop is precisely 0° & 360°

2) Magnitude of the product of open loop gain of amplifier (A) and magnitude of feedback factor β is unity i.e $|A\beta| = 1$

* When $|A\beta|>1$,

The total phase shift is 360° or 0° and $|A\beta|>1$. Then oscillation are of growing type.

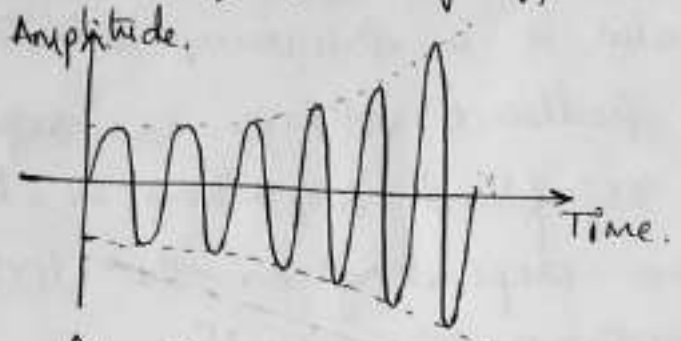


fig: Growing type of oscillations.

* When $|A\beta|=1$.

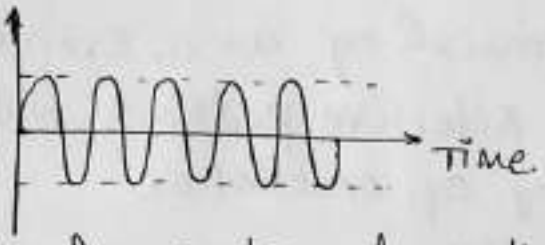


fig: sustained oscillations.

Oscillations with constant frequency and amplitude are called sustained oscillations.

* When $|A\beta|<1$.

The total phase shift is 0° & 360°, $|A\beta|<1$ then the oscillations are of decaying type.

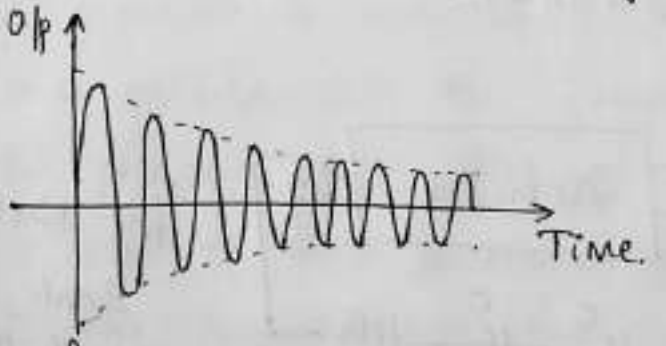


fig: Decaying oscillations.

<u>Note:</u> In practical oscillators, it is not necessary to supply an input signal V_{in} to start oscillations. Instead, oscillations are self-starting and begin as soon as dc power is applied. What makes this possible is thermally produced noise in the resistors and

other components. But only one frequency component fo of the noise satisfies Barkhausen criterion and the circuit oscillates with that particular frequency. i.e feedback nlw is a frequency selector circuit. This initially feedback voltage is amplified and continuously reinforced resulting in buildup of the oscillations depending on the loop gain and the feedback factor of the circuit.

Thus, all practical oscillators have.

1) An Amplifier consisting an active device.
2) A frequency selective feedback nlw to determine the frequency of oscillation.

Phase Shift Oscillator

The figure below shows the Block diagram of Phase shift oscillator.

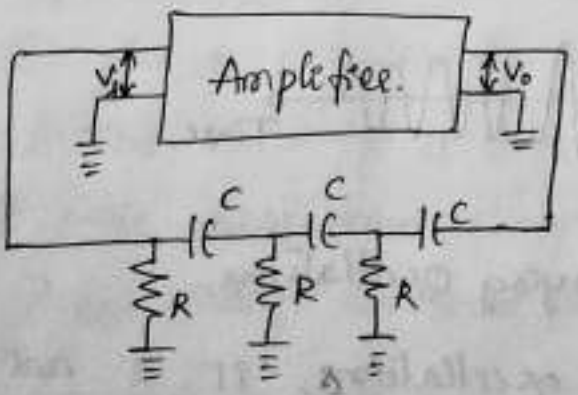


fig: Block diagram of Basic Phase shift oscillator.

This oscillator can be constructed by using Op-Amp and transistor also. with same feedback nlw. This is also called RC-phase shift oscillator. The circuit consists of an amplifier and a feedback nlw consisting

of resistors and capacitors arranged in ladder fashion. Hence such an oscillator is also called ladder type RC phase shift oscillators.

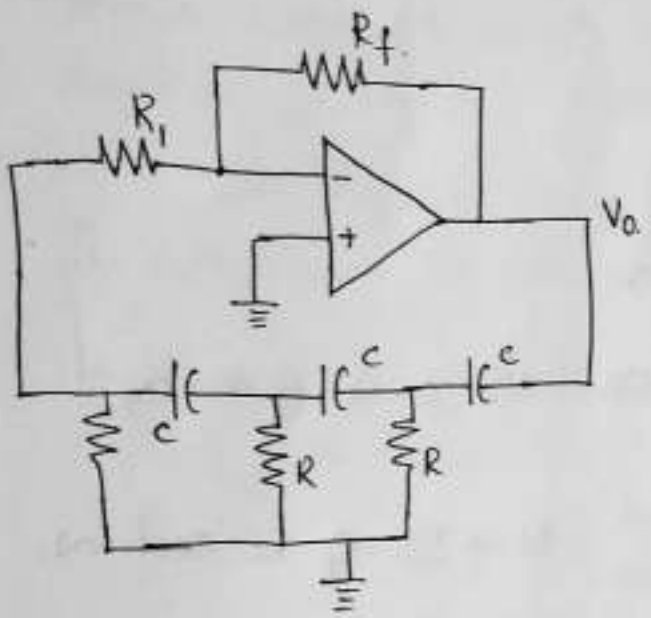


fig: phase shift oscillator using op. Amp.

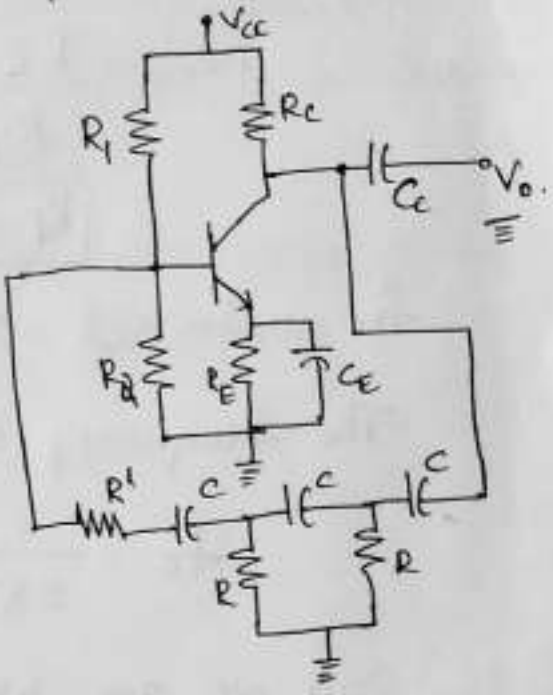


fig: phase shift oscillator using transistor.

Each of the RC sections in the feedback loop can provide a maximum phase shift of 60°. Oscillations occurs at the frequency for which the total phase shift through the 3 RC sections is 180°. The op-Amp is inverting provides 180° to meet the requirement for oscillation of 360° & (0°) phase shift around the loop.

For 3 equal RC sections, the attenuation is

$$\beta = \frac{1}{29} = \frac{V_f}{V_o}$$

To meet the conditions for oscillations i.e Barkhausen's criterion

$|A\beta| = 1 \quad \therefore \quad |A| = 29.$

∴ The voltage gain of the amplifier must be 29.

$$i.e \quad -\frac{R_f}{R_1} = 29.$$

$$\boxed{R_f = 29 R_1}$$

for sustained oscillation.

The frequency of the oscillations is given by.

$$f_o = \frac{1}{2\pi RC\sqrt{2N}} \qquad N \rightarrow \text{no of RC sections.}$$

Since we are using three RC sections.

$$\boxed{f_o = \frac{1}{2\pi RC\sqrt{6}}}$$

Wein Bridge Oscillator

The figure below shows the op-amp based wein bridge oscillator. In order to have more stability and flexibility in changing the frequency wein bridge oscillator is used.

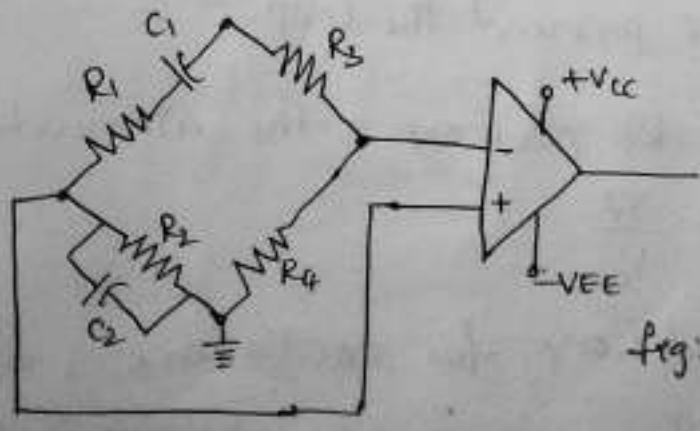


fig: wein bridge oscillator using op-amp.

The feedback nlw comprises of a wein bridge circuit. The op amp is used in non-inverting configuration. Oscillation occurs at the frequency for which the phase shift through the wein bridge is 0° because amplifier is in non-inverting mode.

The figure wein bridge oscillator using Op-Amp can be redrawn as shown in figure below.

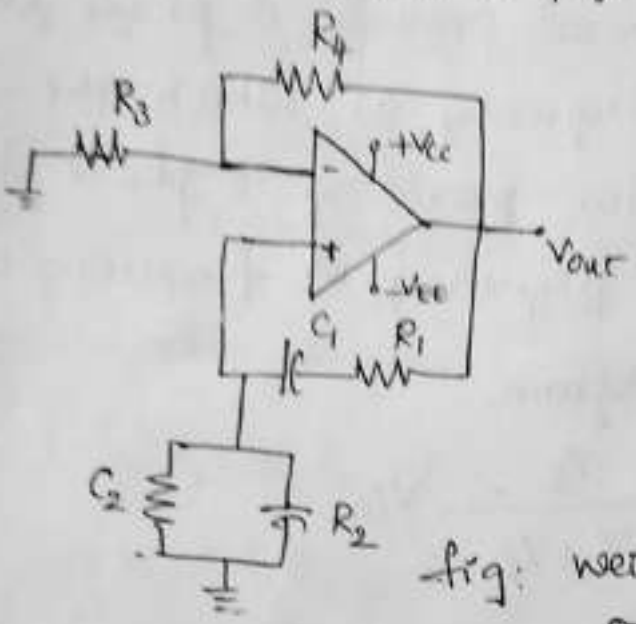


fig: wein bridge oscillator using op-amp.

Derivation for frequency of oscillations for wein bridge

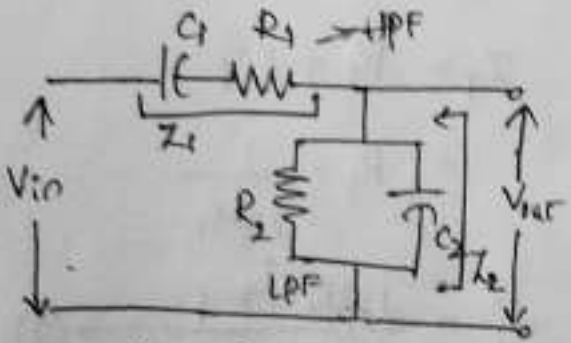
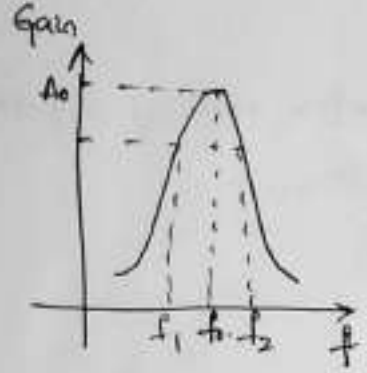


fig: feedback nlw of wein bridge oscillator.

Let us consider feedback nlw of the wein bridge oscillator as shown in fig. which consists of 2RC sections. One RC nlw is connected in series and other RC nlw is connected in parallel. Let us consider the impedance of series RC nlw as Z_1 and impedance of the parallel RC nlw as Z_2.

The Series RC nlw represents High pass filter and parallel RC nlw represents Low pass filter with Low impedance. These both together forms a notch filter. The frequency response of notch filter is as shown below.



The f_o is called the Resonant frequency. as already said the feedback nlw should provide 0° phase shift. The frequency at which the feedback nlw providing 0° phase shift is called Resonant frequency of frequency of Oscillator.

From the circuit diagram,

$$V_{out} = \frac{Z_2}{Z_1+Z_2} \cdot V_{in}$$

$$\Rightarrow \frac{V_{out}}{V_{in}} = \frac{Z_2}{Z_1+Z_2} \longrightarrow (1).$$

$Z_2 = R_2 \| X_{C_2}$

Where $X_{C_2} = \frac{1}{j\omega C_2}$

$Z_2 = R_2 \| 1/j\omega C_2$

$$Z_2 = \frac{R_2 \cdot 1/j\omega C_2}{R_2 + \frac{1}{j\omega C_2}}$$

$$Z_2 = \frac{R_2}{1+j\omega R_2 C_2} \longrightarrow (2)$$

$Z_1 = R_1 + X_{C_1}$

$$= R_1 + \frac{1}{j\omega C_1}$$

$$Z_1 = \frac{j\omega R_1 C_1 + 1}{j\omega C_1} \longrightarrow (3).$$

Substitute the value of Z_1 & Z_2 in eq -(1).

$$\therefore \frac{V_{out}}{V_{in}} = \frac{\frac{R_2}{1+j\omega R_2 C_2}}{\frac{j\omega R_1 C_1 + 1}{j\omega C_1} + \frac{R_2}{1+j\omega R_2 C_2}}$$

$$= \frac{R_2}{1+j\omega R_2 C_2} \times \frac{(j\omega C_1)(1+j\omega R_2 C_2)}{(j\omega R_1 C_1 + 1)(1+j\omega R_2 C_2) + R_2 j\omega C_1}$$

$$= \frac{j\omega R_2 C_1}{j\omega R_1 C_1 + 1 - \omega^2 R_1 C_1 R_2 C_2 + R_2 j\omega C_1 + j\omega R_2 C_2}$$

$$\beta = \frac{V_{out}}{V_{in}} = \frac{j\omega R_2 C_1}{(1-\omega^2 R_1 C_1 R_2 C_2) + j\omega[R_1 C_1 + R_2 C_1 + R_2 C_2]}$$

To find the Resonant frequency, equate

$$1 - \omega^2 R_1 C_1 R_2 C_2 = 0.$$

$$\omega^2 R_1 C_1 R_2 C_2 = 1$$

$$\omega = \frac{1}{\sqrt{R_1 C_1 R_2 C_2}}$$

$$f = \frac{1}{2\pi\sqrt{R_1 C_1 R_2 C_2}}$$

if $R_1 = R_2$ and $C_1 = C_2$

$$\boxed{f = \frac{1}{2\pi\sqrt{RC}}}$$

Therefore, $\beta = \frac{V_{out}}{V_{in}} = \frac{j\omega R_2 C_1}{j\omega[R_1 C_1 + R_2 C_1 + R_2 C_2]}$

$$\beta = \frac{R_2 C_1}{R_1 C_1 + R_2 C_1 + R_2 C_2}$$

$$\beta = \frac{RC}{3RC} \quad [\because R_1 = R_2 = R \ \& \ C_1 = C_2 = C]$$

$$\boxed{\beta = 1/3}$$

$$\beta = \frac{V_{out}}{V_{in}} = \frac{R_2 C_1}{R_1 C_1 + R_2 C_2 + R_2 C_1}$$

for Barkhausen criterion $A\beta = 1$.

$$A = \frac{1}{\beta}$$

$$= \frac{R_1 C_1 + R_2 C_2 + R_2 C_1}{R_2 C_1}$$

$$A = \frac{R_1}{R_2} + \frac{C_2}{C_1} + 1$$

A → Gain of the non inverting amplifier.

$$\therefore \quad 1 + \frac{R_4}{R_3} = \frac{R_1}{R_2} + \frac{C_2}{C_1} + 1.$$

$$\therefore \boxed{\frac{R_4}{R_3} = \frac{R_1}{R_2} + \frac{C_2}{C_1}} \rightarrow \text{This is the}$$

condition to be satisfied for sustained oscillations.

we know $A\beta = 1$. and $\beta = 1/3$.

$$\Rightarrow \underline{\underline{A = 3.}}$$

$$A = 1 + \frac{R_4}{R_3}$$

$$1 + \frac{R_4}{R_3} = 3 \qquad \therefore \frac{R_4}{R_3} = 2$$

$$\Rightarrow \boxed{R_4 = 2R_3}$$

Summarizing we can write.

$$\frac{R_3}{R_4} = \frac{R_1}{R_2} + \frac{C_2}{C_1}$$

$$\therefore \quad f = \frac{1}{2\pi\sqrt{R_1 C_1 R_2 C_2}}$$

If $R_1 = R_2 = R$ & $C_1 = C_2 = C$

$$f = \frac{1}{2\pi RC}$$

and ratio of R_3 to R_4 must be greater than 2 to provide a sufficient loop gain for circuit to oscillate at the frequency.

Problems:

1. Design a RC phase shift oscillator for $f_0 = 1KHz$.

Soln: Given $f_0 = 1KHz$.

For RC phase shift oscillator

$$f_0 = \frac{1}{2\pi\sqrt{6}RC}$$

let $C = 0.1\mu F$. $\therefore R = \frac{1}{2\pi\sqrt{6}C \cdot f}$

$$R = \frac{1}{2\pi\sqrt{6} \times 0.1 \times 10^{-6} \times 1 \times 10^{3}}$$

$$\boxed{R = 650\Omega}$$

$\therefore \frac{R_F}{R} > 29 \Rightarrow R_F > 29R.$

$R_F \geq 29(650)$

$R_F > 18.85K\Omega.$

$\therefore$ Select $R_F = 21K\Omega$

Designed values: $R = 650\Omega$, $R_F = 21K\Omega$. & $C = 0.1\mu F$.

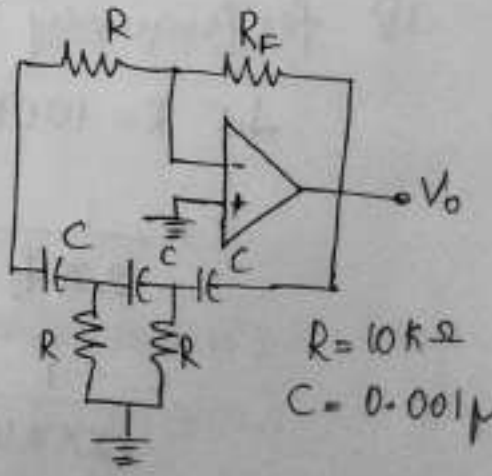
2. a) Determine the value of R_F necessary for the ckt shown in fig. below to operate as an oscillator.
b) what is the frequency of oscillation.

Soln: a) To start oscillation $|A\beta| > 1$

$\beta = \frac{1}{29}$

$\therefore |A| > 29.$

$\frac{R_F}{R} > 29$



$R_F > 29R = 29(10K)$

$R_F > 290K\Omega$.

$\therefore$ Select $\boxed{R_F = 320K\Omega}$

b) Frequency of oscillation: $f_o = \frac{1}{2\pi\sqrt{6}RC}$

$= \frac{1}{2\pi\sqrt{6}(10K)(0.001\mu)}$

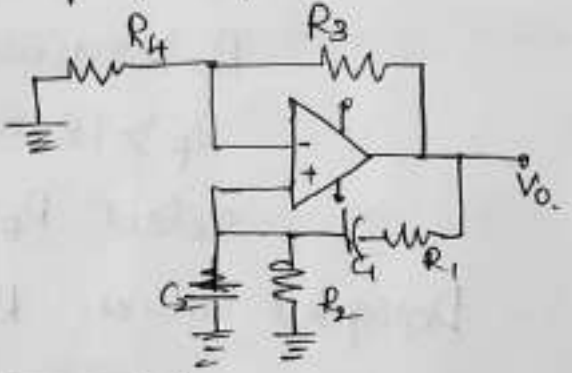
$\boxed{f_o = 6.5\ KHz}$

3) For the ckt shown in fig, $R_1 = R_2 = 61K\Omega$, $C_1 = C_2 = 0.001\mu F$

$R_3 = 300K\Omega$, $R_4 = 100K\Omega$

i) Calculate the frequency of oscillation

ii) Determine the RC values for a frequency of oscillation $f_o = 10KHz$.



Soln: Given: $R_1 = R_2 = R = 61K\Omega$.

i) frequency of oscillation:

$f_o = \frac{1}{2\pi RC} = \frac{1}{2\pi \times 61\times10^3 \times 0.001\times10^{-6}}$

$f_o = 2.609\ KHz$.

ii) for frequency of oscillation: $f_o = 10KHz$.

let $R = 100K\Omega$, then $f_o = \frac{1}{2\pi RC}$

$C = \frac{1}{2\pi f_o R}$

$= \frac{1}{2\pi \times 10\times10^3\times100K} = 0.159nF$.

4) Find the value of R & C for an output frequency of 1 KHz in RC phase shift oscillator.

Soln: Given $f = 1KHz$,

$$f = \frac{1}{2\pi RC\sqrt{6}}$$

let $C = 0.1\mu F$. $\quad R = \frac{1}{2\pi C\sqrt{6}}$

$$R = \frac{1}{2\pi \times 0.1\times 10^{-6}\times \sqrt{6}}$$

$$\boxed{R = 645.74\Omega}$$

5) The frequency of sensitive arms of wein bridge oscillator uses $C_1 = C_2 = 0.001\,\mu F$, $R_1 = 10\,k\Omega$, where R_2 is kept variable. The frequency is to be 10kHz to 60KHz. By varying R_2. Find the min and maximum value of R_2.

Soln: Given $C_1 = C_2 = 0.001\,\mu F$, $R_1 = 10K\Omega$, $f = 10KHz$ to 60kHz

$$f = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}}$$

Case i) $f = 10KHz$.

$$f^2 = \frac{1}{(2\pi)^2(R_1R_2C_1C_2)}$$

$$R_2 = \frac{1}{(2\pi)^2 R_1C_1C_2 \times f^2}$$

$$= \frac{1}{(4\pi^2)(10K)^2(10\times 10^3\times 0.001\times 10^{-6}\times 0.001\times 10^{-6})}$$

$$\therefore \boxed{R_2 = 25.33K\Omega}$$

Case ii) $f = 60Hz$.

$$R_2 = \frac{1}{4\pi^2\times(60\times 10^3)^2\times(10\times 10^3)(0.001\times 10^{-6})\times(0.001\times 10^{-6})}$$

$$\boxed{R_2 = 704.33\Omega}$$

555 Timer

The 555 timer is a popular and versatile monolithic integrated circuit (IC) developed by "signetics corporation" in early 1970. This timer IC is highly stable and generates accurate time delays and oscillations. The time delays and time pulses whose duration and frequency is determined by an externally connected timing resistor and capacitor.

The IC is available in 8 pin and also in 14-pin. This 555 timer can prodive time delays ranging from μs (microseconds) to hours. It requires power supply V_{cc} which can range from +5V to +18V. The 8 pin package is as shown in fig below.

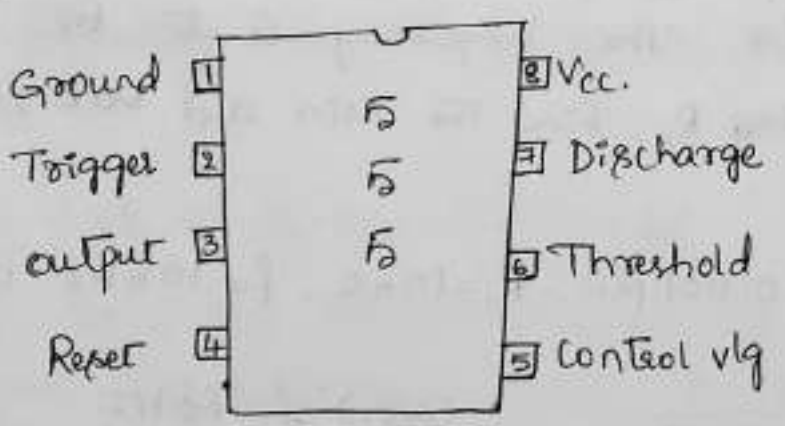


fig: pin diagram of 555 timer.

The below figure shows the internal diagram of the 555 timer. The ckt is divided into 5 parts. 1) voltage divider ckt 2) Comparator made up of two op-amps. 3) Rs flipflop 4) Discharge circuit 5) o/p. The voltage divider consists of three 5k resistors. The comparators are set at 2/3 V_{cc} and 1/3 V_{cc} as reference voltages.

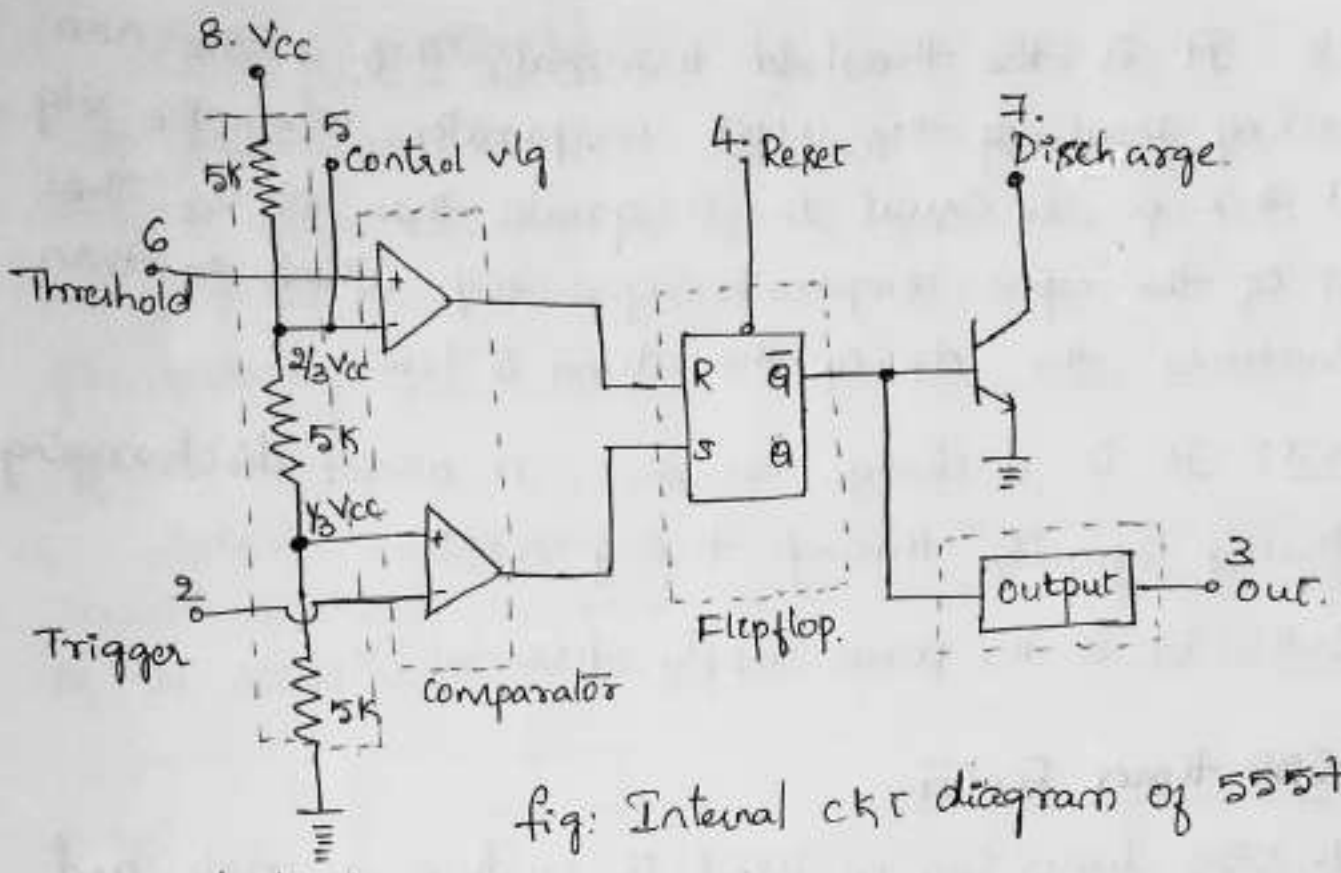


fig: Internal ckt diagram of 555 timer

The following are details of the various pins of 555 timer

Pin 1: It is the ground terminal.

Pin 2: It is the trigger terminal. If the voltage at this terminal is greater than $1/3\ V_{cc}$ the output is Low. Since it is inverting comparator. If the voltage at this terminal is less than $1/3\ V_{cc}$ the O/p is High.

Pin 3: It is the output terminal. This terminal may be High & low.

Pin 4: It is the reset terminal. When not in use it is connected to V_{cc} to avoid any false triggering. The timer can be reset by making this pin Low.

Pin 5: It is the control vlg terminal. An external vlg applied at this pin changes the threshold vlg which is $2/3\ V_{cc}$

Pin 6: It is the threshold terminal. This is the non inverting input of the upper comparator. when the vlg at this pin is equal to of greater than of/3 V_{CC}. Then o/p of the upper comparator goes high which in turn switches the o/p of the timer is low.

Pin 7: It is discharge terminal. It allows discharging timing capacitor through timing resistor.

Pin 8: It is the power supply terminal V_{CC}.

555 timer Features

1. 555 timer can be used to produce accurate and highly stable time delays.
2. It has two operating modes:
   a) Monostable b) Astable.
3. 555 timer can operate with voltage ranging from +5 to +18V and can drive load up to 200 mA.
4. It is compatible with TTL and CMOS logic ckts.
5. Has very high temperature stability [-55° to 120°C].

Applications of 555.

1) Can be used as oscillator
2) Linear ramp generator
3) To generate PWM waves.
4) Frequency divider
5) Automatic Battery-charger.

The two modes of operation of 555 timer is 1) Monostable multivibrator 2) Astable Multivibrator

Astable Multivibrator using IC 555- Timer.

An Astable multivibrator does not have any stable state, it keeps changing its state from low to high and high to low. This type of oscillator is also called free running multivibrator & rectangular wave generator ckt.

Astable multivibrator does not require an external circuit to change the state of the output. The ckt diagram of the Astable multivibrator is as shown in figure below.

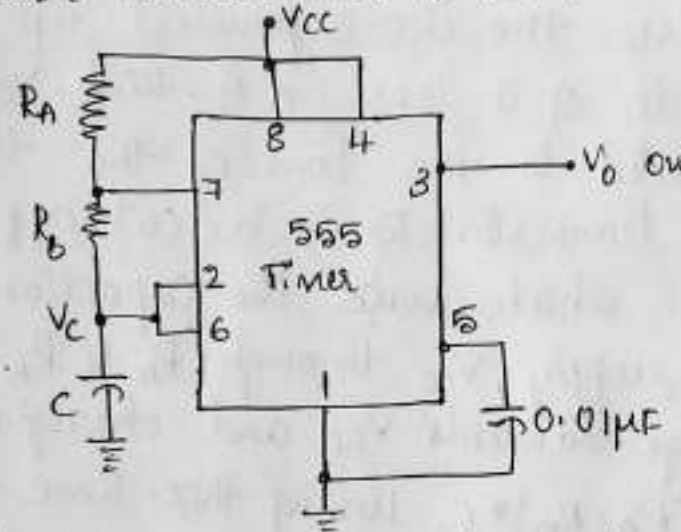


fig: Astable multivibrator using 555 timer.

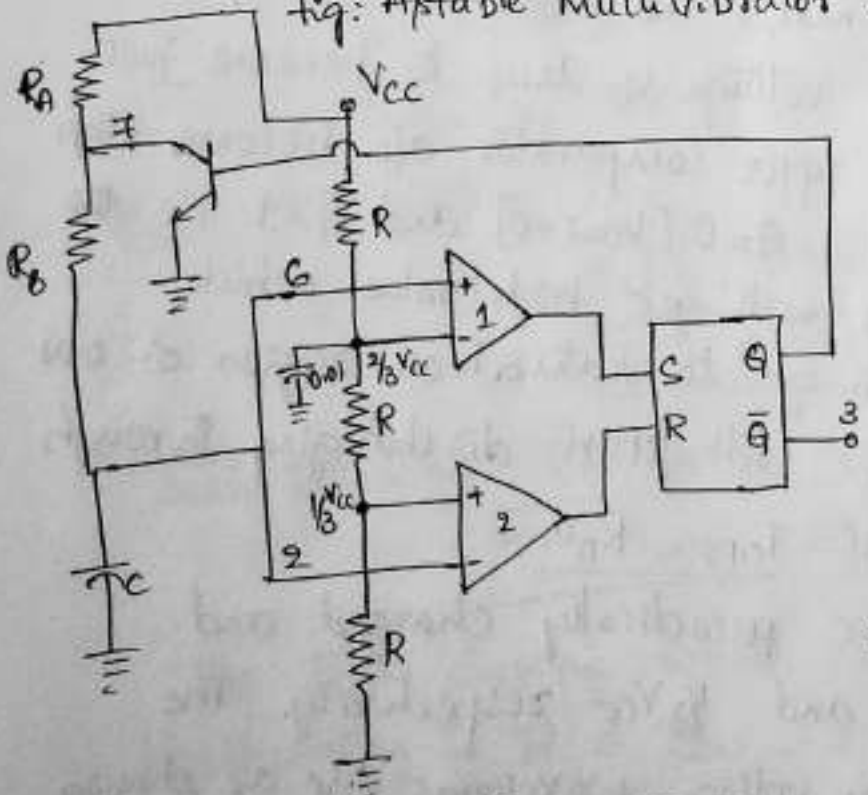


fig: Internal circuitry of 555 Timer

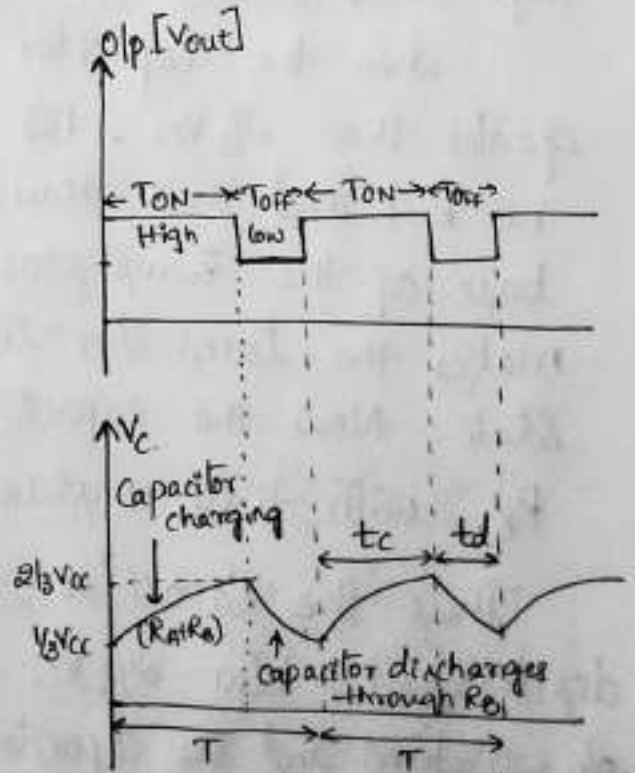


fig: op and capacitor vlg waveform

The Basic objective of an astable multivibrator is to switch the output states at the desired time intervals. without any external intervention. This is achived by controlling the discharge terminal of 555 IC, through a capacitor. Inside the IC, capacitor is connected to the collector of of the transistor whose base is directly connected to the o/p terminal of SR flipflop. Vout is taken from the inverting terminal output (Q) of SR flip flop so when flipflop o/p Q is high Vout will be low and when Q is low. Vout will be high.

Let us assume the ckt is powered up and the states at flipflop is Q is low. i.e $\bar{Q}$ = High [Vout]. The Q is directly connected to the base of the transistor which makes the transistor to be in cut off state [OFF state] i.e open ckt. which makes the capacitor to directly connected to power supply V_{cc} through R_A & R_B. so the Capacitor will charge towards V_{cc} and charging time Constant will be $(R_A+R_B)*C$. During this time output is High. as R=0 and S=1 makes the control FF is $\bar{Q}=0$.

when the capacitor voltage V_c tries to become just greater than $\frac{2}{3}V_{cc}$. the upper comparator o/p becomes high i.e R=1 and S=0 thus Q=0 [Vout=0] and $\bar{Q}=1$ i.e the base of the transistor will get high value which makes the transistor to go to saturation region & ON state. Now the capacitor will start discharging through R_B. with time constant $T_{OFF} = R_B C$.

Thus the Capacitor, C periodically charged and discharged b/w $\frac{2}{3}V_{cc}$ and $\frac{1}{3}V_{cc}$ respectively. The op waveform and the capacitor voltage waveforms are as shown in fig above.

Design:

ON Time: is the time for which the times o/p Vout has remained in High state. It is indicated by T_{ON} & T_{High} & T_C

OFF Time: is the time for which the times o/p Vout has remained in Low state. It is indicated by T_{OFF} & T_{Low} & T_D

ON time and OFF time dependent on the values of R_A R_B and C. So desired ON Time and OFF time can be calculated by R_A & R_B and C values.

* Voltage across the capacitor at any instant during charging period is given by $V_C = V_{cc}(1 - e^{t/Rc})$.
* The time taken by capacitor to charge from 0 to $1/3\ V_{cc}$ is, $1/3 V_{cc} = V_{cc}(1 - e^{t/Rc}) = t_1 = 0.405\ RC$
* The time taken by capacitor to charge from 0 to $2/3 V_{cc}$ is,

$$2/3 V_{cc} = V_{cc}(1 - e^{t/Rc}) = t_2.$$

$$t_2 = Rc \log_e 3 = 1.0986\ Rc$$

∴ time taken by the capacitor to charge from $1/3 V_{cc}$ to $2/3 V_{cc}$ is,

$$T_C = (t_2 - t_1) = (1.0986 - 0.405)\ RC$$

$$\boxed{T_C = 0.693\ RC}$$

Substituting $R = R_A + R_B$.

$$\boxed{T_C = T_{High} = T_{ON} = 0.693(R_A + R_B) * C.}$$

The time during which the capacitor starts discharging is Td & $T_{Low} = 0.693\ R_B C$.

The discharging of capacitor at any instant of time is given by,

$$V_C = \frac{2}{3} V_{CC} \cdot e^{-td/R_B C}$$

Substituting $V_C = \frac{1}{3} V_{CC}$

$$\frac{1}{3} V_{CC} = \frac{2}{3} V_{CC} \cdot e^{-td/R_B C}$$

$$\boxed{td = 0.693 R_B C.} \quad \& \quad \boxed{T_{OFF} = 0.693 R_B C}$$

$\therefore$ Overall period = $T = T_{ON} + T_{OFF}$

$$\boxed{T = 0.693 (R_A + 2R_B) C.}$$

$$\text{Frequency}, f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B) C.}$$

$$\text{Duty cycle} = \frac{T_{High}}{T} = \frac{T_{High}}{T_{High} + T_{LOW}} = \frac{T_{ON}}{T_{ON} + T_{OFF}}$$

$$\text{Duty cycle} = \frac{R_A + R_B}{R_A + 2R_B}$$

$$\boxed{\% \text{ Duty cycle} = \frac{R_A + R_B}{R_A + 2R_B} \times 100}$$

Problems:

1) A 555 timer is connected as astable multivibrator. Given $R_1 = R_2 = 7.5k\Omega$, $C = 0.1\mu F$, $V_{CC} = 5V$ Calculate the frequency of oscillations and sketch the V_{lg} waveform.

Soln:

Given: $R_A = 7.5k\Omega$
$R_B = 7.5k\Omega$
$C = 0.1\mu F$
$V_{CC} = 5V$.

$$T_{ON} = 0.693 (R_A + R_B) * C.$$
$$= 0.693 (7.5 \times 10^3 + 7.5 \times 10^3) * 0.1 \times 10^{-6}$$
$$= 0.693 (15 \times 10^3) \times 0.1 \times 10^{-6}$$

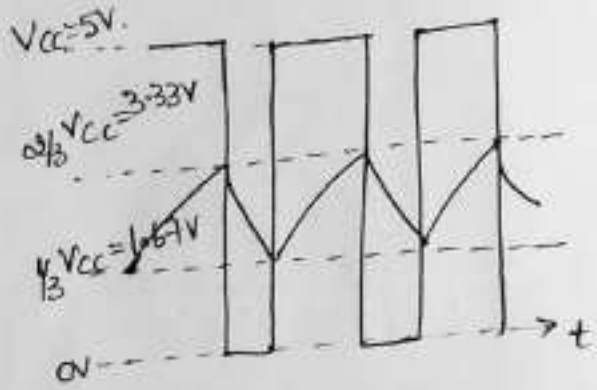
$$\boxed{T_{ON} = 1.04ms}$$

$T_{OFF} = 0.693 R_B \cdot C$

$= 0.693 \times 7.5 \times 10^3 \times 0.1 \times 10^{-6}$

$\boxed{T_{OFF} = 0.52\,ms}$

Waveforms:



Total period, $T = T_{ON} + T_{OFF}$

$= 1.04ms + 0.52ms$

$\boxed{T = 1.56\,ms}$

frequency: $f = \frac{1}{T} = \frac{1}{1.56 \times 10^{-3}}$

$\boxed{f = 640Hz}$

Q) A 555 timer is connected as astable multivibrator for frequency 400KHz. Calculate the value of C if $R_1 = R_2 = 8K\Omega$

Given: $f = 400KHz$

$R_1 = 8K\Omega$

$R_2 = 8K\Omega$

Soln:

$$f = \frac{1.44}{(R_1 + 2R_2)C}$$

$$C = \frac{1.44}{f(R_1 + 2R_2)}$$

$$= \frac{1.44}{400 \times 10^3 (8 + 16) \times 10^3}$$

$\boxed{C = 0.15nf}$

Module-5

Digital Electronics Fundamentals

Digital electronics are the electronics system which use a digital signal instead of analog signal. Analog and digital signals are used to transmit information by means of electrical signals. In both the form, the signal is transformed into electric signals.

Analog signal [continuous time signal]

It is a signal in which, the amplitude of the signal is defined at each and every instant of time. Analog signal process time varying signals that can take any value across continuous range of voltage, current & any physical parameter.

Ex: $V_m \sin\theta$, if $V_m = 20V$

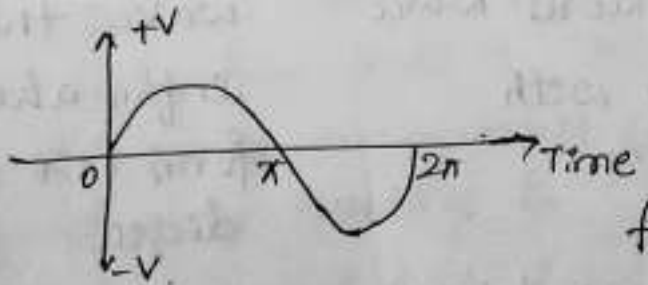


fig: Analog signal.

Digital Signal [Discrete signal]

A digital / digital signal is a one in which the signal is defined only at particular instant of time.

Any continuous signal or analog signal can be converted into Digital signal by a process

Called Sampling. Digital signal is nothing but a sampled version of Analog signal.

In Digital Signals, the information is translated into binary digit (bit) form i.e 0's and 1's where each bit is representing of two distinct amplitudes.

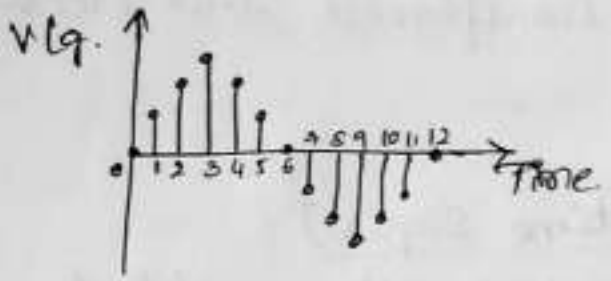


fig: Discrete signal

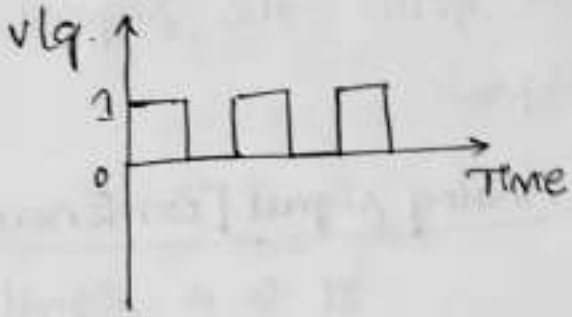


fig: Binary signal.

Difference between Analog & Digital Signal.

Analog Signal	Digital Signals.
1) It is an information carrying continuous wave that changes with respect to time	1) It is the discrete wave that carries information in binary form (i.e 0's & 1's). digit.
2) It is represented by continuous time signals [Sine wave]	2) It is represented by a discrete values of signals. [Square wave]
3) It is described by amplitude, frequency and phase	3) It is described by bit rate & bit intervals.

4) It is more prone to distortion / more susceptible to noise

5) It has no fixed range

6) It transmits data in the form of wave

7) Ex: Human voice, pressure with height.

4) It is less prone to distortion / less susceptible to noise.

5) It has a fixed range.

6) It carries / transmits data in the form of binary form.

7) Ex: Signals used in computer n/ws. and no of accidents occur in one year

Number Systems

The various number systems used in digital systems are.

1) Decimal 2) Binary 3) Octal 4) Hexadecimal.

Decimal Number System:

In Decimal number system only ten numbers are used i.e from 0 to 9. This is called Base-10. System. & radix-10 number system. The general form of decimal number is

$$d_n d_{n-1} \ldots\ldots d_3 d_2 d_1 d_0 . d_1 d_2 d_3 \ldots d_n$$

and its equivalent is given by.

$$d_n \times 10^n + d_{n-1} \times 10^{n-1} + \ldots + d_3 \times 10^3 + d_2 \times 10^2 + d_1 \times 10^1 + d_0 \times 10^0 + d_{-1} 10^{-1} + d_{-2} 10^{-2} + \ldots + d_{-n} \times 10^{-n}$$

For ex: $(2504.189)_{10}$. In this Subscript '10' indicates that the given no is in decimal 10 r/w.

Binary Number System

In a digital electronic system, the active devices used are operated as switches and have only two states i.e ON and OFF. For this reason the binary numbering sys is used in which only 2 digits i.e '0' and 1. So binary number system is base-2 & radix 2 number sys.

The general form of binary number is.

$b_m b_{m-1} b_{m-2} \ldots\ldots b_3 b_2 b_1 b_0 . b_{-1} b_{-2} b_{-3} \ldots\ldots b_n$

and its decimal equivalent is given by.

$b_m \times 2^m + b_{m-1} \times 2^{m-1} + b_{m-2} \times 2^{m-2} + \ldots\ldots + b_3 2^3 + b_2 \times 2^2 + b_1 \times 2^1 + b_0 \times 2^0 + b_{-1} \times 2^{-1} + b_{-2} \times 2^{-2} + \ldots\ldots + b_n \times 2^{-n}$.

for ex: $(11011.1101)_2 = (11011.1101)_b$. The Subscript '2' & 'b' indicates that the given number is in binary & base-2 & radix-2 sys.

(MSB: most significant bit; LSB: least significant bit)

The left most bit of a binary number is called most significant bit (MSB) and the right most bit significant bit (LSB) is called least significant bit (LSB).

Octal Number System:

Decimal number is most commonly used and it is most since we are using it in everyday life transactions. and binary numbers are important because binary numbers can be processed directly using digital sys.

Radix 8 of octal number sys is it is not used directly but they are important for documentation and other purposes. It provides shorthand representation of multibit numbers in a digital sys. The octal sys needs 8 digits i.e 0 to 7.

The general form of octal number is,

$O_m O_{m-1} O_{m-2} \ldots\ldots O_3 O_2 O_1 O_0 O_{-1} O_{-2} O_{-3} \ldots\ldots O_{-n}$

and its equivalent decimal is,

$O_m \times 8^m + O_{m-1} \times 8^{m-1} + \ldots\ldots + O_3 \times 8^3 + O_2 \times 8^2 + O_1 \times 8^1 + O_0 \times 8^0 + O_{-1} \times 8^{-1}$

$+ O_{-2} \times 8^{-2} + O_{-3} \times 8^{-3} + \ldots\ldots + O_{-n} \times 8^{-n}$

for ex: $[736.56]_0 = [736.56]_8$. The subscript 8 of 0 indicates that the given number is octal number.

Hexdecimal Number system:

This number system is not commonly used. This is used to shorten the representation of multibit numbers in a digital sys. It is also called Radix-16 of Hexdecimal number sys. The hexdecimal number sys it is not used much. But it provides shorthand representation of multiber numbers in a digital sys.

The Hexadecimal number system has 15 digits of numbers. i.e 0 to 9 and A to F.

The gneral form of hexdecimal number is

$H_m H_{m-1} H_{m-2} \ldots\ldots H_3 H_2 H_1 H_0 . H_{-1} H_{-2} H_{-3} \ldots\ldots H_n$

and its decimal equivalent is given by,

$$H_m \times 16^m + H_{m-1} \times 16^{m-1} + H_{m-2} \times 16^{m-2} + \ldots\ldots + H_3 \times 16^3 + H_2 \times 16^2 + H_1 \times 16^1 + H_0 \times 16^0 + H_{-1} \times 16^{-1} + H_{-2} \times 16^{-2} \ldots\ldots + H_n \times 16^{-n}$$

Ex:

$(ABC.D)_{16} = (ABC.D)_H$. The subscript '16' & 'H' indicates that the given number is in Hexdecimal number & base-16 & radix-16 s/m.

Number Conversions

I. Decimal to Any base - 'r' s/m.

Let us consider a decimal number which has both integer and fractional part. The integer part is converted into base 'r' s/m by successive division and writing the remainders respectively. The remainders are to be written in sequence from "bottom to top".

The fractional part is converted into base 'r' s/m by successive multiplication by 'r' and writing the whole part of the result. The sequence to be from top to bottom. The multiplication to be continued until the fractional part becomes zero. or desired accuracy is obtained.

ex: 1) $(398.75)_{10}$ to binary.

In the given number 398 is a integer part and 0.75 is the fractional part.

2 | 398	
2 | 149 - 0	
2 | 74 - 1	
2 | 37 - 0	
2 | 18 - 1	
2 | 9 - 0	
2 | 4 - 1	
2 | 2 - 0	
1 - 0	

0.75×2
$1.50 \longrightarrow 1$
0.50×2
$1.00 \longrightarrow 1$

$(0.75) = (0.11)$.

$398 = (100101010)$

$\therefore (398.75)_{10} = (100101010.11)_2$.

2) $(398.75)_{10}$ to octal i.e base-8.

8 | 398	
8 | 49 - 6	
6 - 1	

0.75×8
$6.00 \longrightarrow 6$

$(398)_{10} = 616$

$[398.75]_{10} = [616.6]_8$.

3) $(398.75)_{10}$ to Hexdecimal.

16 | 398	
16 | 24 - 14(E)	
1 - 8	

0.75×16
$12.00 \longrightarrow 12(C)$

$[398.75]_{10} = [18E.C]_H$

Examples:

1) $(734)_{10}$ to binary.

2	734
2	367 – 0
2	183 – 1
2	91 – 1
2	45 – 1
2	22 – 1
2	11 – 0
2	5 – 1
2	2 – 1
	1 – 0

$(734)_{10} = (1011011110)_2$

2) Convert $(1010.101)_{10}$ into binary.

2	1010.
2	505 – 0
2	252 – 1
2	126 – 0
2	63 – 0
2	31 – 1
2	15 – 1
2	7 – 1
2	3 – 1
	1 – 1

0.101×2
$0.202 \rightarrow 0$

0.202×2
$0.404 \rightarrow 0$

0.404×2
$0.808 \rightarrow 0$

0.808×2
$1.616 \rightarrow 1$

0.616×2
$1.232 \rightarrow 1$

$(1010.101)_{10} = (1111110010.00011\ldots)_2$

3) Convert $(8899)_{10}$ into hexadecimal.

16	8899
16	556 – 3
16	34 – C
	2 – 2

$(8899)_{10} = (22C3)_H$.

4) $(0.368)_{10}$ into Hexadecimal.

Soln:

$0.368 \times 16 = 5.888$

$0.888 \times 16 = E.208$

$0.208 \times 16 = 3.328$

$0.328 \times 16 = 5.248$

$0.248 \times 16 = 3.968$

$\vdots$

$(0.368)_{10} = (0.5E353)$.

5) perform the following $(2003)_{10} = (\quad)_8$.

8	2003	
8	250	— 3
8	31	— 2
8	3	— 7
	0	— 3

$(2003)_{10} = (3723)_8$.

6) Convert $(0.705)_{10}$ into octal.

$0.705 \times 8 = 5.64$

$0.64 \times 8 = 5.12$

$0.12 \times 8 = 0.96$

$0.96 \times 8 = 7.68$

$0.68 \times 8 = 5.44$

$\vdots$

$(0.705)_{10} = (0.5\,5\,0\,7\,5)_8$.

II. Any base 'r' to Decimal.

Here we have to use the general rule for representing numbers in any number system.

$$a_n a_{n-1} \ldots a_2 a_1 a_0 = a_n r^n + a_{n-1} r^{n-1} + \ldots + a_2 r^2 + a_1 r^1 + a_0 r^0$$

1) $(110111)_2 = (\ ?\ )_{10}$

$$(110111)_2 = 1\times2^5 + 1\times2^4 + 0\times2^3 + 1\times2^2 + 1\times2^1 + 1\times2^0$$
$$= 32 + 16 + 0 + 4 + 2 + 1$$
$$= (55)_{10}.$$

2) $(11101.1011)_2 = 1\times2^4 + 1\times2^3 + 1\times2^2 + 0\times2^1 + 1\times2^0 + 1\times2^{-1} + 0\times2^{-2} + 1\times2^{-3} + 1\times2^{-4}$

$$= 16 + 8 + 4 + 0 + 1 + 1/2 + 0 + 1/8 + 1/16$$
$$= (29.6875)_{10}.$$

3) $(0.011011)_2 = 0\times2^{-1} + 1\times2^{-2} + 1\times2^{-3} + 0\times2^{-4} + 1\times2^{-5} + 1\times2^{-6}.$

$$= 0 + \frac{1}{4} + \frac{1}{8} + \frac{0}{} + \frac{1}{32} + \frac{1}{64}$$
$$= 0 + 0.25 + 0.125 + 0.03125 + 0.015625$$
$$= (0.421875)_{10}.$$

4) $(10001101)_2 = 1\times2^7 + 0\times2^6 + 0\times2^5 + 0\times2^4 + 1\times2^3 + 1\times2^2 + 0\times2^1 + 1\times2^0$

$$= 128 + 0 + 0 + 0 + 8 + 4 + 1$$
$$= (141)_{10}.$$

5) $(476.25)_8 = (?)_{10}$

$(476.25)_8 = 4\times8^2 + 7\times8^1 + 5\times8^0 + 2\times8^{-1} + 5\times8^{-2}$

$= 256 + 56 + 5 + 2\cdot 1/8 + 5\times 1/64$

$= (317.32813)_{10}$.

6) $(9B2.1A)_H = (?)_{10}$

$(9B2.1A)_H = 9\times16^2 + B(11)\times16^1 + 2\times16^0 + 1\times16^{-1} + A(10)\times16^{-2}$

$= 2304 + 176 + 2 + 1\cdot 1/16 + 10\cdot 1/256$

$= 2304 + 176 + 2 + 0.0625 + 0.039$

$= (2482.1)_{10}$.

7) $(3102.12)_4 = (?)_{10}$

$= 3\times4^3 + 1\times4^2 + 0\times4^1 + 2\times4^0 + 1\times4^{-1} + 2\times4^{-2}$

$= 192 + 16 + 0 + 2 + 1/4 + 2\cdot 1/16$

$= (210.375)_{10}$.

8) $(614.15)_7 = (?)_{10}$.

$= 6\times7^2 + 1\times7^1 + 4\times7^0 + 1\times7^{-1} + 5\times7^{-2}$

$= 294 + 7 + 4 + 1/7 + 5\cdot 1/49$

$= 294 + 7 + 4 + 0.142857 + 0.102$

$= (305.24486)_{10}$.

9) $(ABC.D)_{16} = (?)_{10}$

$= A(10)\times16^2 + B(11)\times16^1 + C(12)\times16^0 + D(13)\times16^{-1}$

$= 2560 + 176 + 12 + 0.8125$

$= (2748.8125)_{10}$.

III Binary to Octal Conversion.

Octal number	Binary Number
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

* For binary to octal number conversion of whole number, group the given binary number in groups of those three starting from the right most [LSB] and replace each group by the octal number. shown in the above table.
* For conversion of fractional part, make group of three starting with the left most bit. If any of the bit is left alone add zeros to make a group of three towards right side of the number.

ex: 1) $(101111)_2 = (\ ?\ )_8$

$\underline{101}\ \underline{111} = (57)_8$

2) $(1110.01101)_2 = (?)_8$

$\underline{001}\ \underline{110}.\ \underline{011}\ \underline{010}$

$= (16.32)_8$.

3) $(1111011011011.11011)_2 = (?)_8$.

001 111 011 011 011. 110 110 $= (17333.66)_8$

4) $(1110110110.11101)_2$

011 011 011 10. 111010 $= (3556.75)_8$.

5) $(0.11110101101)_2 = (?)_8$

0. 111 101 011 010 $= (7532)_8$

IV. Octal to Binary Conversion

To convert octal to binary, simply replace each octal number by its equivalent 3 bit binary number.

1) $(724)_8 = (?)_2$

$724 = (111\,010\,100)_2$

2) $(365.217)_8 = (?)_2$

$365.217 = (011\,110101.010\,001\,111)_2$

3) $(0.506) = (0.101\,000\,110)_2$

4) $(7463.245)_8 = (111\,100\,110\,011.\,010\,100\,101)_2$

V. Binary to Hexdecimal Conversion

Hex decimal	Binary.
0	0000
1	0001
2	0010
3	0011
4	0100

5 - 0101
6 - 0110
7 - 0111
8 - 1000
9 - 1001

(A) 10 - 1010
(B) 11 - 1011
(C) 12 - 1100
(D) 13 - 1101
(E) 14 - 1110
(F) 15 - 1111

* For binary to hexadecimal conversion of whole number. group the given binary number in groups of those four starting from the right most [LSB] and replace each groups by the hexadecimal no shown in above figure.

* For conversion of fractional part, make group of four starting with the left most bit. If any of the bit is left alone add zeros to make a group of four towards right side of the number.

ex:

1) $(110111101.01)_2 = (?)_{16}$.

$\underline{0001}\,\underline{0111}\,\underline{1101}.\underline{0100} = (1BD.4)_{16}$.

2) $(1101111010111101)_2$

$\underline{0110}\,\underline{1111}\,\underline{0101}\,\underline{1101} = (6F5D)_{16}$.

3) $(0.1101010111011)_2$

$0.\underline{1101}\,\underline{0101}\,\underline{1101}\,\underline{1000} = (0.D5D8)_{16}$.

VI. Hexadecimal to Binary Conversion.

To convert hexadecimal to binary, simply replace each hexadecimal by its equivalent of binary using 4 bits.

ex: 1) $(ABC)_{16} = (1010\ 1011\ 1100)_2$.

2) $(777)_H = (0111\ 0111\ 0111)_2$

3) $(2AB.9)_{16} = (?)_2$

$= (0010\ 1010\ 1011.1001)_2$

4) $(22E.7E8)_{16} = (?)_2$

$(22E.7E8)_H = (0010\ 0010\ 1110.0111\ 1110\ 1000)_2$.

VII. Octal to Hexadecimal Conversion

To convert octal to Hexadecimal number. we cannot convert directly therefore octal numbes should be first converted into binary and then convert into Hexadecimal number. i.e

Octal → Binary number → Hexadecimal numbes.

ex: 1) $(437)_8 = (?)_{16}$.

$(437)_8 = 100\ 011\ 111 = 000100011111$

$= (11F)_{16}$.

2) $(726.627)_8 = (?)_{16}$.

$(726.627)_8 = 111\ 010\ 110 . 110\ 010\ 111$

$= 0001\ 1101\ 0110 . 1100\ 1011\ 1000$

$= (1D6.CB8)_{16}$.

3) $(16.2)_8 = (?)_{16}$

$(16.2)_8 = 001\ 110 . 010$

$= 0000\ 1110 . 0100.$

$= (0E.4)_{16}$

4) $(0.76)_8 = (?)_{16}$.

$(0.76)_8 = 0.\ 111\ 110$

$= 0.11111000 = (0.F8)_{16}$.

VIII. Hexadecimal to octal number.

To convert hexadecimal to octal number is not possible directly. So first convert the number into binary then to octal number by grouping 3 bits together. and write its Octal equivalent.

Hexadecimal ⟶ Binary ⟶ octal number.

ex: 1) $(777)_H = (?)_8$.

$(777)_H = (0111\,0111\,0111) = (3567)_8$.

2) $(22E.7E8)_H = (?)_8$.

$(22E.7E8)_H = (0010\,0010\,1110.\,0111\,1110\,1000)$

$= (1056.3750)_8$.

Summary of Conversion Methods.

Conversion	Method.
1) Binary to Decimal	Multiply by 2 with respective powers
2) Octal to Decimal	Multiply by 8
3) Hexdecimal to Decimal	Multiply by 16.
4) Decimal to binary	Divide whole number by 2 and multiply fraction by 2.
5) Decimal to octal	Divide whole number by 8 and multiply fraction by 8.
6) Decimal to Hexdecimal	Divide whole number by 16 and multiply by 16 of the fraction.
7) octal to Binary	representing each digit by group of 3-bits.

8) Binary to octal - grouping into 3 bits

9) Hexadecimal to Binary - represent each digit by group of 4-bits.

10) Binary to Hexadecimal - grouping into 4-bits.

11) Octal to Hexadecimal - Octal → binary → Hexadecimal.

12) Hexdecimal to octal - Hexadecimal to binary to octal.

Problems:

1) Convert $(284.65)_{10} = (?)_8 = (?)_{16} = (\quad)_2$.

2	284	
2	142	0
2	71	0
2	35	1
2	17	1
2	8	1
2	4	0
2	2	0
	1	0

$(284.65)_{10} = (100011100.101\ldots)_2$.

0.65×2
$1.30 \rightarrow 1$

0.30×2
$0.60 \rightarrow 0$

0.60×2
$1.20 \rightarrow 1$

$(284.65)_{10} = (11C.A\ldots)_{16}$

$(284.65)_{10} = (434.5146)_8$.

2) $(532.65)_{10} = (?)_{16} = (?)_2$

16	532	
16	33	4
	2	1

0.65×16
$10.4 \rightarrow 10$

0.4×16
$6.4 \rightarrow 6$

0.4×16
$6.4 \rightarrow 6$.

$(532.65)_{10}$
$= (214.A66)_{16}$.
$= (0010\ 0001\ 1000.1010\ 0110\ 0110)_2$.

3) $(ABCD)_{16} = (\quad)_2 = (\quad)_8$

$(ABCD)_{16} = (1,010\ ,101,1\ \ 11,00\ 1,101)_2$

$= (125715)_8$

4) perform the following.

a) $(57.6)_8 = (?)_2 = (?)_{16}$

$(57.6)_8 = (101111.110)_2$

$= (2F.C)_{16}$

5) $(193)_{16} = (?)_8 = (?)_{10}$

$(193)_{16} = 0001\ 1001\ 0011$

$(193)_{16} = (623)_8$

$(193)_{16} = 1\times16^2 + 9\times16^1 + 3\times16^0 = (403)_{10}$

6) Convert $(526.44)_8 = (?)_2 = (?)_{10}$

$(526.44)_8 = (101010110.100100)_2$

$(526.44)_8 = 5\times8^2 + 2\times8^1 + 6\times8^0 + 4\times8^{-1} + 4\times8^{-2}$

$= (342.5625)_{10}$

7) Convert i) $(2AB.8)_{16} = (?)_{10} = (?)_8$

$(2AB.8)_{16} = 2\times16^2 + A(10)\times16^1 + B(11)\times16^0 + 8\times16^{-1}$

$= (683.5)_{10}$

$(2AB.8)_{16} = 0010\ 1010\ 1011\ .\ 1000$

$= (1253.40)_8$

$(2AB.8)_{16} = (683.5)_{10} = (1253.40)_8$.

ii) $(764.352)_8 = (?)_{16} = (?)_2$

$(764.352)_8 = (111\ 110\ 100.\ 011\ 101\ 010)_2$

$= (1F4.750)_{16}$.

$(764.352)_8 = (111110100.011\ 101010)_2 = (1F4.75)_H$.

8) Convert the following.

i) $(101010.101)_2 = (?)_{10}$.

$101010.101 = 1\times 2^5 + 0\times 2^4 + 1\times 2^3 + 0\times 2^2 + 1\times 2^1 + 0\times 2^0 + 1\times 2^{-1} + 0\times 2^{-2} + 1\times 2^{-3}$

$= (42.625)_{10}$.

ii) $(7034)_8 = (?)_{10}$.

$= 7\times 8^3 + 0\times 8^2 + 3\times 8^1 + 4\times 8^0$

$= (3612)_{10}$.

iii) $(2616)_{10} = (?)_{16}$.

$(2616)_{10} = (A38)_{16}$.

16 | 2616
16 | 163 – 8
10 – 3

iv) $(934)_{10} = (?)_8$.

$(934)_{10} = (1646)_8$.

8 | 934
8 | 116 – 6
8 | 14 – 4
1 – 6

9) Determine the value of x

i) $(183)_x = (312)_7$.

$1\times x^2 + 8\times x^1 + 3\times x^0 = 3\times 7^2 + 1\times 7^1 + 2\times 7^0$

$x^2 + 8x + 3 = 147 + 7 + 2$

$x^2 + 8x + 3 = 156$

$x^2 + 8x - 153 = 0$

$(x+17)(x-9) = 0$

$\therefore x = -17$ & $x = 9$

Base cannot be negative number.

$\therefore \boxed{x = 9}$

2) $(211)_x = (152)_8$

$2 \times x^2 + 1 \times x^1 + 1 \times x^0 = 1 \times 8^2 + 5 \times 8^1 + 2 \times 8^0$

$2x^2 + x + 1 = 64 + 40 + 2$

$2x^2 + x + 1 = 106$

$2x^2 + x - 105 = 0$

$\therefore x = 7$ & $x = -15/2$

$\therefore \boxed{x = 7}$

3) $(303)_x = (457)_8$

$3 \times x^2 + 0 \times x + 3 \times x^0 = 4 \times 8^2 + 5 \times 8^1 + 7 \times 8^0$

$3x^2 + 3 = 256 + 40 + 7$

$3x^2 - 300 = 0$ $\quad x = \pm 10$

$x^2 - 100 = 0$ $\quad \therefore \boxed{x = 10}$

4) $(1323)_x = (523)_8$

$1 \times x^3 + 3 \times x^2 + 2 \times x + 3 \times x^0 = 5 \times 8^2 + 2 \times 8^1 + 3 \times 8^0$

$x^3 + 3x^2 + 2x + 3 = 320 + 16 + 3$

$x^3 + 3x^2 + 2x - 300 = 0$

$x_1 = 6, \; x_2 = -4.5, \; x_3 = -4.5$

$\therefore \boxed{x = 6}$

Complements

For a given number 'N' in base-r, we can define two types of complements.

i) r's complement ii) (r-1) complement.

Therefore a decimal number (r=10) has 10's complement and 9's complement. A Binary number has 2's complement and 1's complement. octal number (8=r) has 8's complement and 7's complement. Hexadecimal (r=16) has 16's complement and 15's complement.

The r's complement of a number may be obtained by leaving all least significant zeros unchanged, subtracting the first non-zero least significant digit from 'r' and then subtracting all other higher significant digits from r-1.

The (r-1)'s complement of a number may be obtained by subtracting all digits from (r-1).

BINARY ADDITION

There are four basic cases of binary addition.

1) $0+0=0$ 3) $1+0=1$

2) $0+1=1$ 4) $1+1=10$ [Carry = 1 and Sum = 0]

Ex: ① Add 13 & 10.

first convert the Decimal no to Binary and then perform addition

i.e $(13)_{10} = 1101$

$\underline{(10)_{10} = 1010}$

$(23)_{10} \quad (10111)_2$.

② Add $(3.25)_{10}$ and $(5.75)_{10}$.

i.e $(3.25)_{10} = (11.01)_2$

$\underline{(5.75)_{10} = (101.11)_2}$

$9.00 \quad (1001.00)_2$.

Binary Subtraction.

There are four basic cases of binary subtraction.

$0-0=0$. $\quad 0-1=1$ (10)

$1-0=1$ $\quad 1-1=0$

ex: $1101 - 1010 \Rightarrow$

$$\begin{array}{r} 1101 \\ 1010 \\ \hline 0011 \end{array}$$

Subtraction can be done in two ways ① using i's complement & ② using 9's complement.

I. Using i's complement

The i's complement of any binary number is obtained by changing each 0's to the number by 1 and each 1's in the number by a 0.

Ex: ① 1001 — i's complement is 0110.

d) 11010111 → 1's complement is 00101000.

Subtraction using 1's complement.

There are two cases.

Case: i) When the Subtrahand (the number to be subtracted) is smaller than the minuend.

procedure:

1) Get the 1's complement of subtrahand.
2) Add it with minuend.
3) If carry present add it to the LSB of the result. Answer is +ve.

Case: ii) when the Subtrahand (the number to be subtracted) is greater than the minuend.

procedure:

1) Get the 1's complement of the subtrahand.
2) Add it with the minuend.
3) The carry will be zero. & if carry is not generated take 1's complement of the result and place "a negative sign with result"

examples:

1) $(1101)_2 - (1000)_2 = (?)_2$

Taking 1's complement of subtrahand 1000 = 0111

Add it with minuend.

i.e 1101
0111

Carry → 1 0100
↳ 1

0101 ← result.

$\therefore \boxed{(1101)_2 - (1000)_2 = (0101)}$

2) 110010 − 101101

1's complement of 101101 → 010010.

```
     110010
   + 010010
   --------
carry → 1|000100
          └────→1
   --------
     000101 → Result
```

(110010) − (101101) = 000101.

3) 1101011 − 1110101.

1's complement of 1110101 → 0001010.

```
    1101011
  + 0001010
  ---------
    1110101
Carry=0.
```

No carry generated. ∴ Take the 1's complement of the result i.e − 0001010.

∴ **1101011 − 1110101 = − 0001010**

4) $(11101)_2 - (11000)_2 = (?)_2$

```
        11101 ← Minuend
        00111 ← 1's complement of subtrahend
       ------
Carry = 1|00100
          └────→1
       ------
        00101 ← Result.
```

$(11101)_2 - (11000)_2 = 00101.$

5) $(11000)_2 - (11101)_2 = (?)_2$

11000 ← Minuend
00010 ← 1's complement of subtrahend
Carry=0 11010

No carry generated ∴ Take the 1's complement of the result i.e -00101

∴ $(11000)_2 - (00010)_2 = -00101$

Subtraction using 2's complement

2's complement: To find the 2's complement first find one's complement then add 1 to the L.S.B of the 1's complement. ex: 1011 → 0100 ← 1's complement, +1, 0101 ← 2's complement.

Subtraction using 2's complement:

1) Determine the 2's complement of subtrahend
2) Add it with Minuend.
3) If there is a carry, discard it. Answer is +ve.
4) If there is no carry, Answer is negative. Taking 2's complement of the result and place a -ve sign with the result.

ex: 1. 1101 - 1010.

Soln: 1's complement — 0101, +1, 0110 ← 2's complement.

1101
0110
10011 ← Carry discard

∴ Result = $(0011)_2$.

2) 110001 − 110101

```
  110001
  001011
  ------
  111100   No carry.
```

001010
+1
001011 ← 2's complement

take 2's complement of the result.

i.e. 000011
+1
−(000100)$_2$

110001 − 110101 = −000100

3). 1101 − 1010.

```
   1101
   0110
  -----
 1|0011
```

carry = 1 discard

0101
+1
0110 ← 2's complement

∴ 1101 − 1010 = 0011

Add the following using 2's complement.

1) $(125)_{10} - (68)_{10}$.

$125 = (1111101)_2$

$68 = (1000100)_2$

2	125
2	62 − 1
2	31 − 0
2	15 − 1
2	7 − 1
2	3 − 1
	1 − 1

2	68
2	34 − 0
2	17 − 0
2	8 − 1
2	4 − 0
2	2 − 0
	1 − 0

```
   1111101
   0111100
  --------
 1|0111001
```

↑ discard carry.

0111011
+1
0111100 ← 2's compliment.

$(0111001)_2 = (57)_{10}$.

$(1111101)_2 - (1000100)_2 = (0111001)_2$

$(125)_{10} - (68)_{10} = (57)_{10}$.

Boolean Algebra

A Boolean algebra is a set of binary operations addition, subtraction and multiplication with elements 0 & 1 such that the following laws hold.

Rules in Boolean Algebra

1) $0+0=0$, $0+1=1$ $\Rightarrow 0+A=A$ & $A+0=A$.

2) $1+0=1$, $1+1=1$ $\Rightarrow 1+A=A$ & $A+1=A$.

3) $0+0=0$, $1+1=1$ $\Rightarrow A+A=A$.

4) $0+1=1$, $1+0=1$ $\Rightarrow A+\bar{A}=1$

5) $0\cdot 0=0$, $0\cdot 1=0$ $\Rightarrow 0\cdot A=0$.

6) $0\cdot 1=0$, $1\cdot 0=0$ $\Rightarrow A\cdot\bar{A}=0$

7) $1\cdot 0=0$, $1\cdot 1=1$ $\Rightarrow 1\cdot A=A$.

8) $0\cdot 0=0$, $1\cdot 1=1$ $\Rightarrow A\cdot A=A$.

9) $\bar{\bar{0}}=0$, $\bar{\bar{1}}=1$ $\Rightarrow \bar{\bar{A}}=A$.

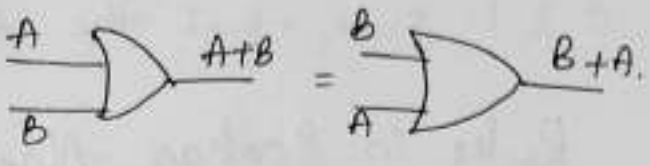
Properties of Boolean Algebra. [Boolean Laws]

1) Commutative property
2) Distributive property
3) Associative property
4) Demorgon's Law.
5) Absorption law:

1) Commutative property.

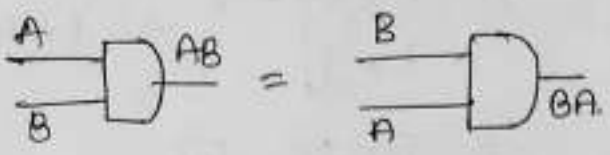
a) $A+B = B+A$.

A	B	A+B	B+A
0	0	0	0
0	1	1	1
1	0	1	1
1	1	1	1



b) $AB = BA$.

A	B	AB	BA
0	0	0	0
0	1	0	0
1	0	0	0
1	1	1	1

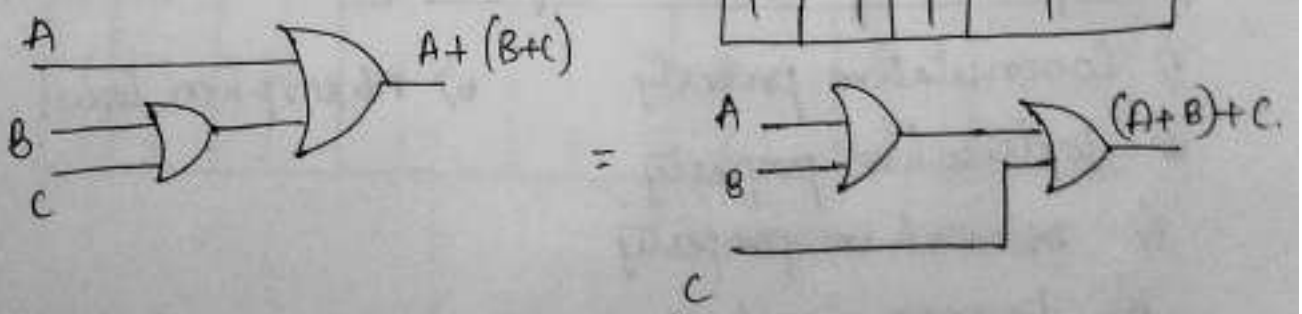


2) Associative property.

a) $A+(B+C) = (A+B)+C$.

A	B	C	A+B	(A+B)+C
0	0	0	0	0
0	0	1	0	1
0	1	0	1	1
0	1	1	1	1
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

A	B	C	A+(B+C)
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

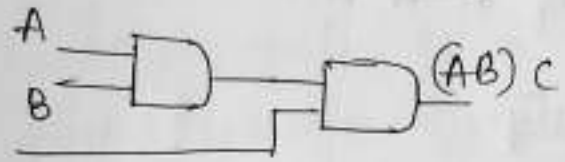


b) $(AB)C = A(BC)$

A	B	C	AB	(AB)C
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	0	0
1	0	0	0	0
1	0	1	0	0
1	1	0	1	0
1	1	1	1	1

=

A	B	C	BC	A(BC)
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	1	0
1	0	0	0	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1



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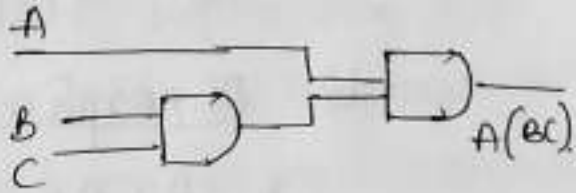
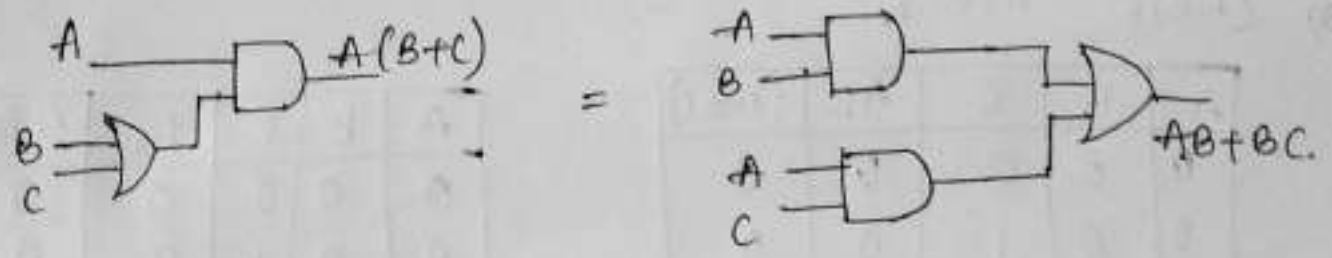


3) Distributive Property

a) $A(B+C) = AB + AC$

A	B	C	B+C	A(B+C)	AB	BC	AB+BC
0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	1	0	0	0	0
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	1	1	1	0	1	1
1	1	0	1	1	1	0	1
1	1	1	1	1	1	1	1

$A(B+C) = AB + BC$.



4) Duality property.

a) Complement property.

$A \cdot \bar{A} = 0$; $A + \bar{A} = 1$.

* The complement of 0 is 1, the complement of 1 is 0.
* The complement of A is $\bar{A}$.

b) Absorption property.

* $A + AB = A$.
* $A(A + B) = A$.

c) Idempotency property.

* $A + A = A$ * $A \cdot A = A$.

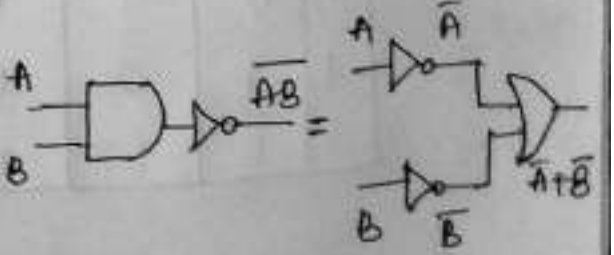
This law refers to the property of sameness.

Demorgan's Theorem.

1) $\overline{AB} = \bar{A} + \bar{B}$.

The complement of the product will be equal to the sum of the complements.

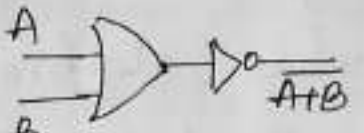
A	B	$\overline{AB}$	$\bar{A} + \bar{B}$
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

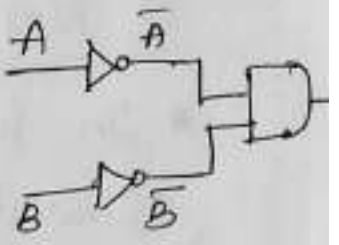


9) $\overline{A+B} = \bar{A}\ \bar{B}$

The complement of a sum is equal to the product of the complements.

A	B	$\overline{A+B}$	$\bar{A}\cdot\bar{B}$
0	0	1	1
0	1	0	0
1	0	0	0
1	1	0	0





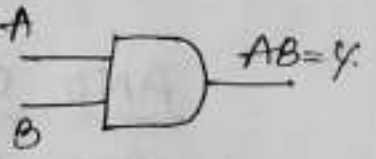
LOGIC GATES

Logic gate is a logic ckt with one o/p & two & more i/p's. The o/p signal is produced when there is a specific combination of i/p signals.

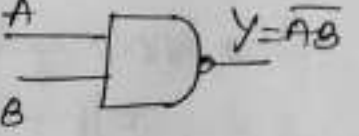
* Only NOT gate has one i/p

The various types of Gates are.

1) NOT : 

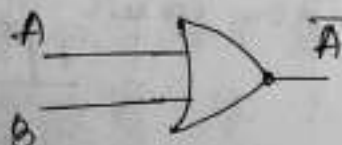
3) AND : 

2) OR : 

4) NAND : 

5) E-XOR : 

6) EX-NOR : 

7) NOR 

Basic Boolean Logic Operations.

1) AND Operation (Logical Multiplication).
2) OR operation [Logical Addition]
3) NOT Operation [Logical complementary].

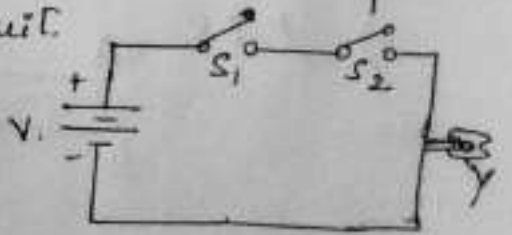
* In Boolean algebra the constants & variables are allowed to have only two possible values 0 & 1. Other terms used for representing 0 & 1 are as follows:

0	1
logic 0	logic 1
False	True
OFF	ON
Low	High
Open switch	closed switch
NO	YES

AND Operation:

* AND Operation is represented by AND gate.
* AND gate has two & more inputs and a single o/p
* AND gate is an electronic circuit in which all the i/p's must be High in order to have High o/p.

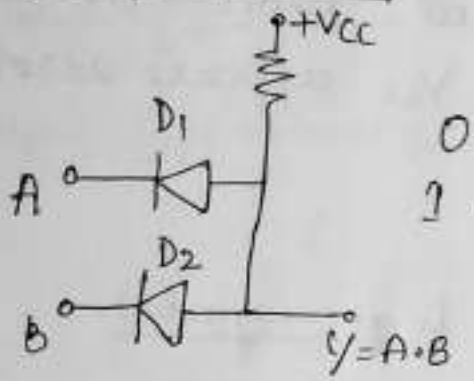
The AND gate / AND function can be explained by following series switching circuit.



Input		o/p (y)
S_1	S_2	
open	open	OFF
open	close	OFF
close	open	OFF
close	close	ON

* The Lamp will glow only if the switches A & B are simultaneously ON.

The Diode Logic for an AND gate is shown in figure below.



0 → 0V
1 → 5V.

Truth table for 2 i/p.

Inputs		output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

fig: Logic ckt for AND using Diodes.

Case i) When A=0V & B=0V.

When both input A & B are low voltages, the Cathodes of both the diodes are grounded. The Diodes get forward biased & hence they conduct & the o/p voltage becomes zero.

Case ii) When A=0 & B=1 (high).

* Since A is low (grounded), the +ve supply v/g Vcc forward biases the Diode D_1 and the Diode D_1 conducts hence the o/p v/g becomes zero.
* Diode D_2 is reverse biased hence it does not conduct and, o/p is zero. (Low)

Case iii) When A=1 and B=0.

* Since voltage B is low (grounded). The +ve supply voltage V_{cc} forward biases the Diode D_2 &

the diode D_2 conducts. Hence the o/p v/g is zero.

* Diode D_1 is reverse biased, hence it does not conducts. o/p is zero (LOW).

Case iv) when A=1 & B=1.

When both voltages A & B are high (+5V) both diodes get reverse biased, hence the diode D_1 & D_2 do not conduct. There Vcc appears across o/p i.e o/p becomes High.

Timing Diagram:

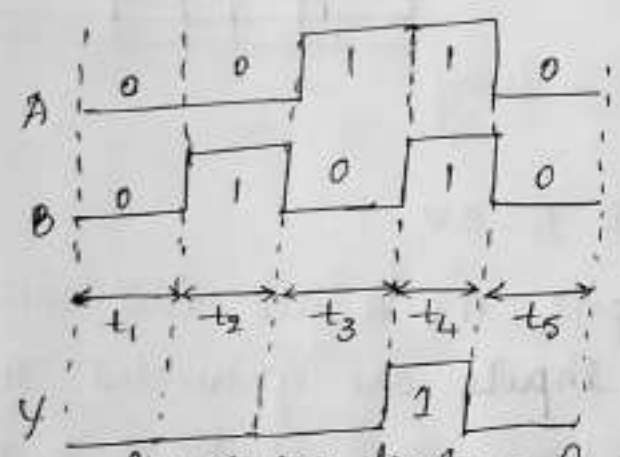
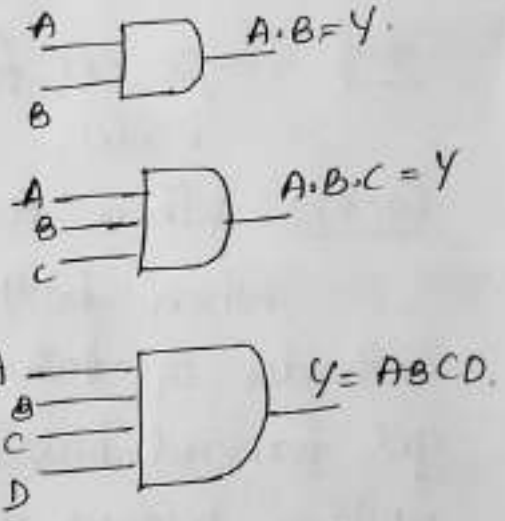


fig: timing diagram for 2i/p AND gate.

Logic Symbol.



OR Gate:

* The o/p of an OR gate is High if any one i/p is High & more i/p's have one. The OR function can be explained by the following ckt.

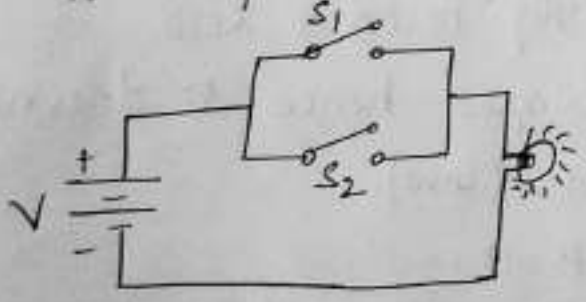
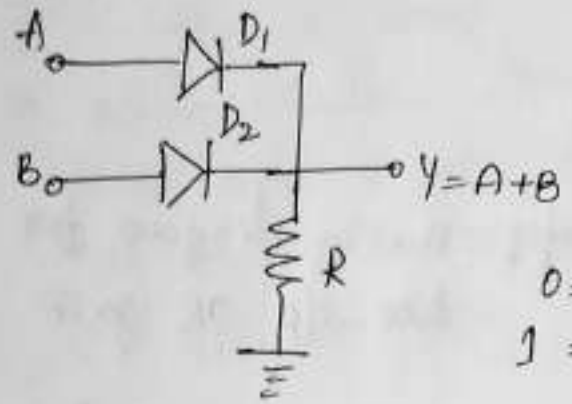


fig: Electrical ckt representation of OR gate.

Inputs S_1	Inputs S_2	o/p = Y. [Lamp]
open	open	OFF
open	close	ON
close	open	ON
close	close	ON

The circuit consists of a battery, a lamp & 2 parallel switches S_1 & S_2 if any one of the switch is closed then the lamp glows.

The Diode circuit for 2 I/p OR gate is given by.



0 = 0V
1 = 5V.

Inputs A	Inputs B	output Y
0	0	0
0	1	1
1	0	1
1	1	1

2-i/p OR gate.

* if Any one of I/p is high i.e 5V. The o/p will be high.

Case i): When A=0 & B=0.

Both diodes are not conducting and hence o/p=0.

Case ii) when A=0 & B=1.

Diode D_1 does not conduct, D_2 diode will conduct. ∴ o/p Y is high.

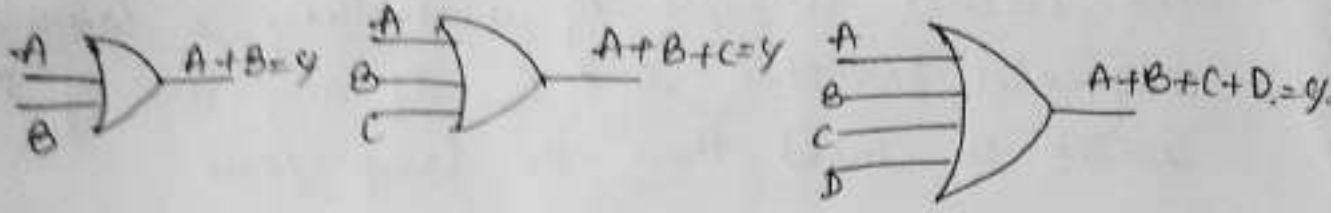
Case iii) When A=1 & B=0:

Diode D_1 conducts and diode D_2 does not conduct. ∴ o/p Y is High.

Case iv) : When A=1 and B=1.

Both diodes are forward biased ∴ o/p Y is High. i.e Y= 5V. [High].

The symbol for 2-i/p. 3-i/p and 4-i/p are as shown in fig.



Timing Diagram

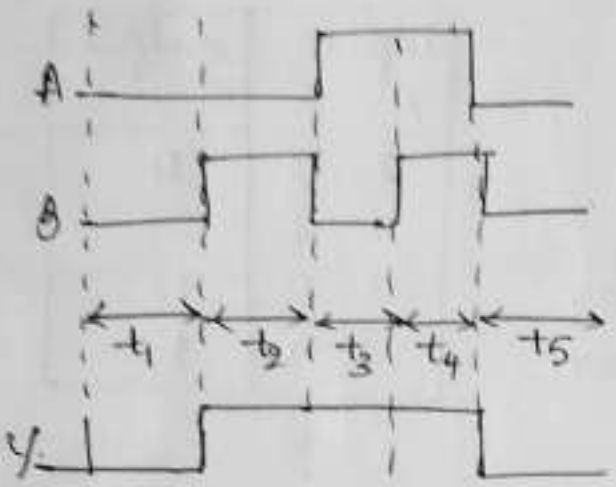
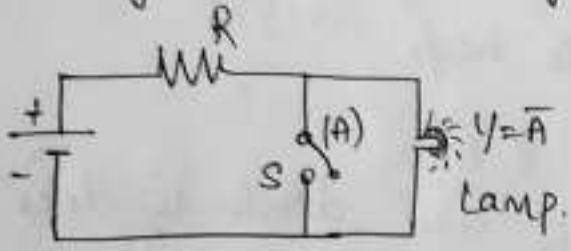


fig: Timing diagram for two I/p OR gate

NOT Gate:

* A gate that performs the mathematical operation of taking the complement is called a NOT Gate.
* A NOT circuit has a single I/p & single O/p. NOT gate can be analysed by the circuit below.



I/p	O/p
Switch open (Low)	LAMP ON. (High)
Switch close (High)	Lamp OFF (Low).

* When switch A is open bulb glows. ∵ current will flow through the lamp.
* When switch A is closed, all the current flows through short circuit & bulb will be OFF.

Realization of NOT gate using transistor.

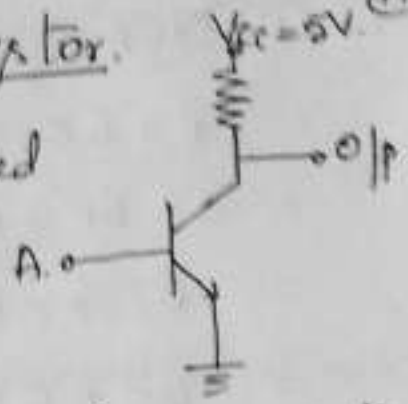
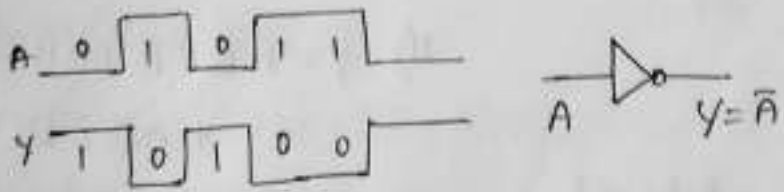


fig: NOT gate using transistor.

* when A is High, transistor is turned ON & acts as a short ckt. Thus entire V_{cc} flows to ground.
  ∴ O/p is Low.
* when A = Low, transistor is turned OFF & acts as a open ckt. Thus the entire V_{cc} appears across the O/p.
  ∴ O/p is High.

Timing Diagram



output of an inverter for pulse i/p.

Simplify the following Boolean Expressions.

1) $A + AC = A(1+C)$
$= A.$

2) $A + \bar{A}B + AB\bar{C}$
$= A(1 + B\bar{C}) + \bar{A}B$
$= A \cdot 1 + \bar{A}B$
$= (A + \bar{A})(A+B)$
$= A + B.$

3) $A + \bar{A}B + ABC + A\bar{C}$
$= A(1 + BC + \bar{C}) + \bar{A}B$
$= A \cdot 1 + \bar{A}B$
$= A + \bar{A}B$
$= (A + \bar{A})(A+B)$
$= A + B.$

4) $\bar{A}C + \overline{AC}$
$= \bar{A}C + \bar{A} + \bar{C}$
$= \bar{A}(C+1) + \bar{C}$
$= \bar{A} + \bar{C}.$

5) $(B+\bar{C})(\bar{B}+C) + \overline{\bar{A}+B+\bar{C}}$

$= B\bar{B} + \bar{B}\bar{C} + BC + C\cdot\bar{C} + A\bar{B}C$

$= 0 + \bar{B}\bar{C} + BC + 0 + A\bar{B}C$

$= \bar{B}\bar{C} + C(B + A\bar{B})$

$= \bar{B}\bar{C} + C(B+A)(B+\bar{B})$

$= \bar{B}\bar{C} + C(B+A)\cdot 1$

$= \bar{B}\bar{C} + BC + AC.$

6) $\overline{\bar{A}+\bar{B}+\bar{C}}$

$= \overline{(\bar{A}+\bar{B})}\cdot\bar{\bar{C}}$

$= (A+B)C$

$= AC + BC.$

7) $\overline{A\bar{B} + \bar{A}\bar{B} + A}$

$= \overline{A\bar{B}}\cdot\overline{AB}\cdot\bar{A}$

$= 0.$

8) $A\bar{B} + \bar{A} + \overline{A\bar{B}}$

$= A\bar{B} + \bar{A} + \bar{A} + \bar{B}$

$= A\bar{B} + \bar{A} + \bar{B}$

$= A\bar{B} + \overline{A\bar{B}}$

$= 1.$

9) $Y = A\bar{B} + AB.$

$= A(\bar{B}+B)$

$= A.$

10) $Y = ab + ac + bd + cd$

$= a(b+c) + d(b+c)$

$= (b+c)(a+d)$

$Y = (b+c)(a+d).$

11) $Y = \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}C\bar{D} + A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}D.$

$= \bar{B}\bar{C}(\bar{A}\bar{D} + \bar{A}D + A\bar{D} + AD)$

$= \bar{B}\bar{C}[\bar{A}(\bar{D}+D) + A(\bar{D}+D)]$

$= \bar{B}\bar{C}[A + \bar{A}]$

$= \bar{B}\bar{C}\cdot 1$

$= \bar{B}\cdot\bar{C}$

12) $F = B(A+C) + C$

$= AB + BC + C$

$= AB + C(1+B)$

$= AB + C$

13) $F = (A+B)BC + A.$

$= ABC + BC + A.$

$= A(1+BC) + BC$

$= A + BC.$

14) $F = A\bar{B}(B+C)$

$= A\bar{B}\cdot B + A\bar{B}C$

$= 0 + A\bar{B}C$

$F = A\bar{B}C.$

15) $F = B[(A+B')(B+C)]$

$= B[AB + AC + BB' + B'C]$

$= AB + ABC + 0 + 0$

$= AB(1+C)$

$F = AB$

16) $abc[ab + c'(bc+a)]$

$= abc[ab+0]$

$= abc.$

17) $ab + \bar{a}\bar{c} + a\bar{b}c(ab+c)$

$= ab + \bar{a}\bar{c} + a\bar{b}c.ab + a\bar{b}c.c$

$= ab + \bar{a}\bar{c} + 0 + a\bar{b}c$

$= a(b + \bar{b}c) + \bar{a}\bar{c}$

$= a(b+\bar{b})(b+c) + \bar{a} + \bar{c}$

$= a(b+c) + \bar{a} + \bar{c}$

$= (\bar{a}+a)(\bar{a}+b) + (\bar{c}+c)(\bar{c}+a)$

$= \bar{a} + b + \bar{c} + a$

$= 1 + b + \bar{c}$

$= 1.$

18) $[wx + wy'](x+w) + wx(x+y)'$

$= wx + wy' + wx + wxy' + wxx' + wxy'$

$= wx(1+y'+x') + wy'(1+x)$

$= wx + wy'$

$= w(x+y').$

19) $\bar{A}C + \overline{AC}$

$= \bar{A}C + \bar{A} + \bar{C}$

$= \bar{A}(1+C) + \bar{C}$

$= \bar{A} + \bar{C}.$

* Prove the following.

1) $(A+C)(A+D)(B+C)(B+D) = AB + CD.$

$LHS = (A+C)(A+D)(B+C)(B+D)$

$= (A + AC + AD + CD)(B + BC + BD + CD)$

$= AB + ABC + ABD + BCD + ABC + ABC + ABCD + ABD + ABCD + ABD + ACD + ACD + ACD + CD.$

$= AB + ABC + ABD + ACD + CD + ABCD.$

$= AB(1+C+D) + ACD + CD + ABCD.$

$= AB + CD(1+A) + ABCD.$

$= AB(1+CD) + CD$

$= AB + CD. = R.H.S$

Simplify the following Boolean functions to a minimum number of literals.

1) $f = x + x'y$.

$= (x + x')(x + y)$

$= x + xy + x'y$

$= x + y(x + x')$

$f = x + y$.

2) $f = x'y'z + x'yz$.

$= x'z(y' + y)$

$= x'z \cdot 1$

$= x'z$

3) $xyz + x'y + xyz'$

$= xy(z + z') + x'y$

$= y(x + x')$

$= y$.

4) $xz + x'xy$

$= x(x + x'y)$

$= x(x + x')(x + y)$

$= x(x + y)$

5) $y(wz' + wz) + xy$.

$= wyz' + wyz + xy$.

$= wy(z + z') + xy$.

$= y(w + x)$.

6) $ABC + A'B'C + A'BC + ABC' + ABC'$

$= BC(A + A') + A'B'(C + C') + ABC'$

$= BC + A'B' + ABC'$

$=$

$= B(C + AC') + A'B'$

$= B(A + C) + A'B'$

7) $[(CD)' + A]' + A + CD + AB$

$= [(\overline{CD}) \cdot \bar{A}] + A + CD + AB$ [Using DeMorgan's Theorem]

$= [CDA'] + A + CD + AB$.

$= CD(A' + 1) + A(1 + B)$

$= CD + A$.

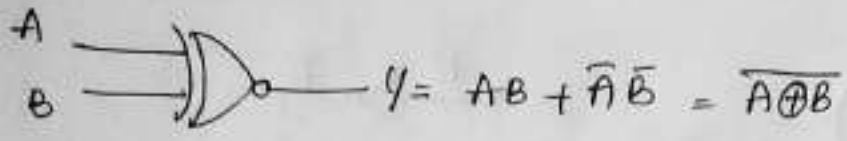
8) $a'b + a'bc' + a'bcd + a'bc'd'e$

$= a'b[1 + c' + cd + c'd'e]$

$= a'b$.

Exclusive NOR Gate [X-NOR]

Negative of XOR gate is XNOR gate. The xNOR o/p is low when the i/p's have odd number of 1's.



$Y = \overline{A \oplus B}$

w.k.r $A \oplus B = A\bar{B} + \bar{A}B$

$= \overline{A\bar{B} + \bar{A}B}$

$= (\overline{A\bar{B}})(\overline{\bar{A}B})$

$= (\bar{A} + \bar{\bar{B}})(\bar{\bar{A}} + \bar{B})$

$= (\bar{A} + B)(A + \bar{B})$

$= A\bar{A} + AB + \bar{A}\bar{B} + B\cdot\bar{B}$

$\boxed{Y = AB + \bar{A}\bar{B}}$

A	B	Y = A ⊙ B
0	0	1
0	1	0
1	0	0
1	1	0

Basic Gates :-

All boolean expressions consists of various combinations of the basic expressions OR, AND & NOT. Any expressions can be implemented using AND, OR, & NOT Gates.

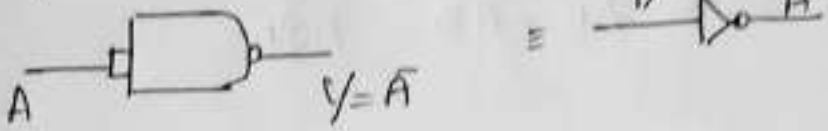
UNIVERSAL GATES:

NAND & NOR Gates are called universal gates because it is possible to implement all the logic expressions using only NAND & NOR gates.

BASIC Gates Using NAND Gates

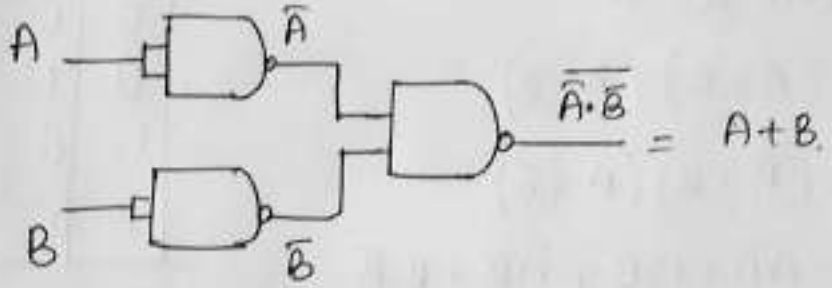
1. NOT Gate

$Y = \bar{A}$

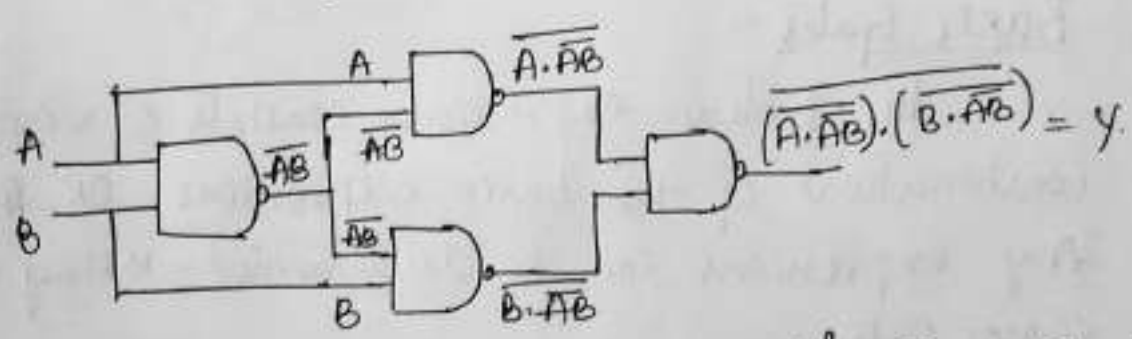


2. AND Gate

3. OR Gate



4. XOR Gate : $Y = A \oplus B$



$$Y = \overline{(A\cdot\overline{AB})\cdot(B\cdot\overline{AB})}$$

$$= \overline{(A\cdot\overline{AB})} + \overline{(B\cdot\overline{AB})}$$

$$= (A\cdot\overline{AB}) + (B\cdot\overline{AB})$$

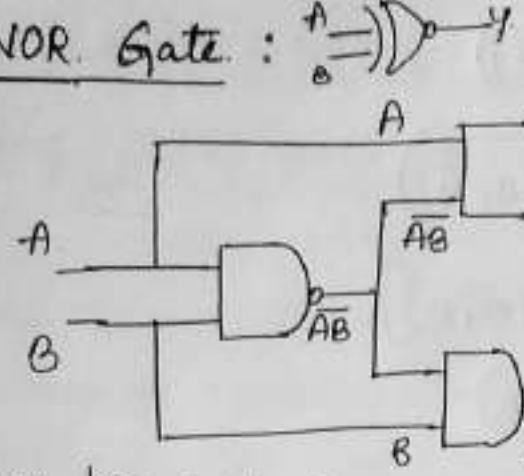
$$= A(\bar{A}+\bar{B}) + B(\bar{A}+\bar{B})$$

$$= A\bar{A} + A\bar{B} + B\cdot\bar{A} + B\bar{B}$$

$$= A\bar{B} + B\cdot\bar{A}$$

$$\boxed{Y = A \oplus B}$$

5) XNOR Gate :



We know that.

$$A \odot B = \overline{A \oplus B}$$

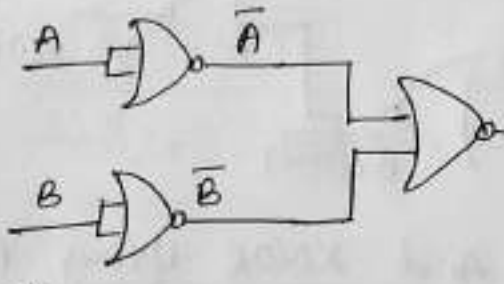
$$= \overline{A}\overline{B} + AB.$$

BASIC Gates Using NOR Gates

1) NOT Gate.

$= \overline{A}\cdot\overline{A} = \overline{A} = Y.$

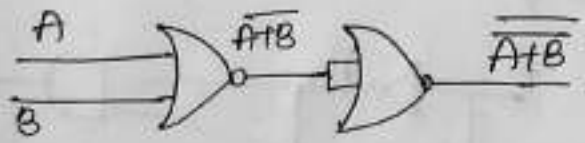
2) AND Gate



$= \overline{\overline{A}}\cdot\overline{\overline{B}}$

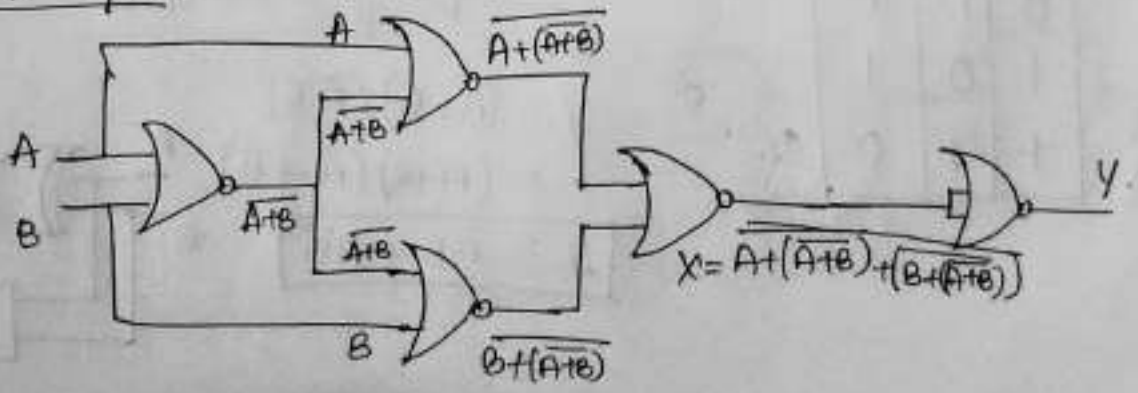
$Y = AB.$

3) OR Gate



$= Y = A+B.$

4) XOR Gate



$$X = \overline{\left(\overline{A + \overline{(A+B)}}\right) + \left(\overline{B + \overline{(A+B)}}\right)}$$

$$= \left(\overline{\overline{A + \overline{(A+B)}}}\right) \cdot \left(\overline{\overline{B + \overline{(A+B)}}}\right)$$

$$= \left[A + \overline{(A+B)}\right] \cdot \left[B + \overline{(A+B)}\right]$$

$$= \left[A + (\bar{A} \cdot \bar{B})\right]\left[B + \bar{A}\bar{B}\right)$$

$$= AB + \bar{A} \cdot B\bar{B} + A \cdot \bar{A}\bar{B} + \bar{A}\bar{B}$$

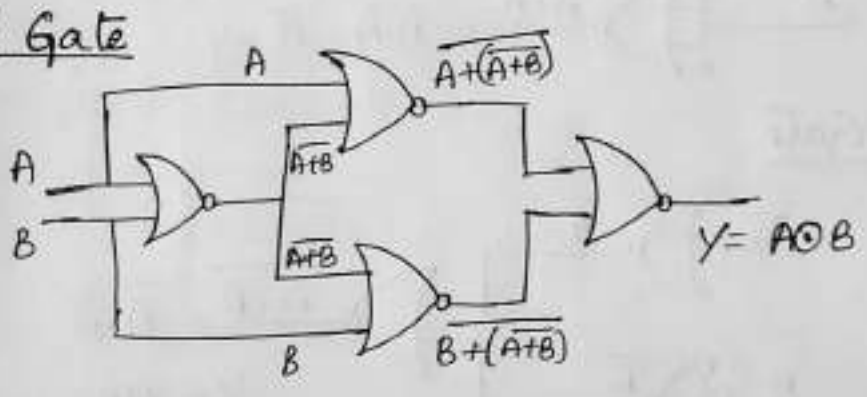
$$X = AB + \bar{A}\bar{B}$$

$$= A \odot B$$

$$X = A \odot B$$

$X' = Y$; i.e $A \odot B = A \oplus B$.

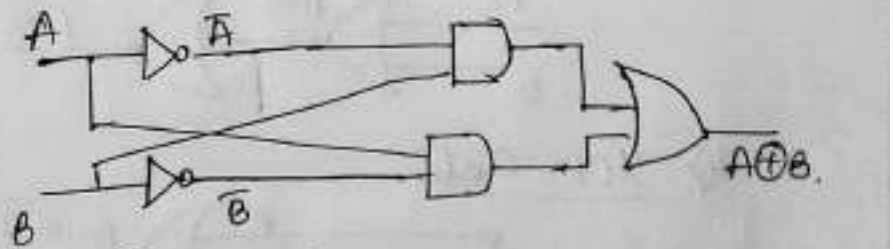
5) XNOR Gate



Realization of XOR and XNOR using Basic Gates

1) XOR = $A\bar{B} + \bar{A}B = Y$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

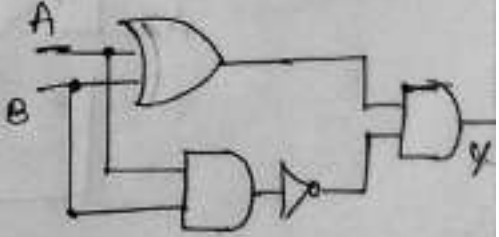


&

$Y = (A+B)(\overline{AB})$

$= (A+B)(\bar{A}+\bar{B})$

$\boxed{Y = \bar{A}B + A\bar{B}}$



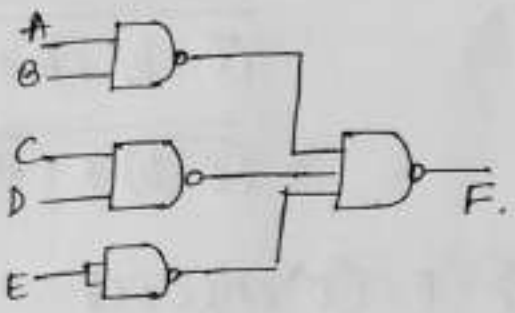
Boolean Functions using Universal Gates

1) **Using NAND gates only:** To implement Boolean function using NAND gates only. it is to be brought to the sum of product (SOP) form and then apply De-Morgan's theorem twice. For example, $F = AB + CD + E$ (function in SOP form).

Applying De-Morgan's Law

$$\overline{\overline{F}} = \overline{\overline{AB + CD + E}}$$

$$= \overline{\overline{AB} \cdot \overline{CD} \cdot \overline{E}}$$



1) $F = (A + \overline{B})(CD + E)$

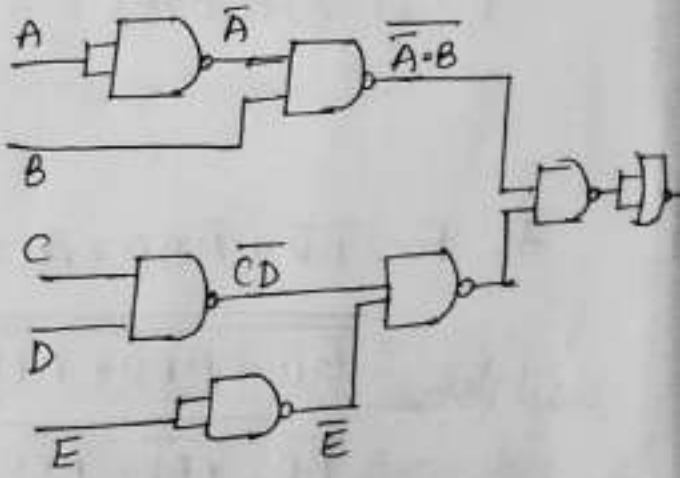
$$= \overline{\overline{(A+\overline{B})(CD+E)}}$$

$$= \overline{\overline{(A+\overline{B})} + \overline{(CD+E)}}$$

$$= \overline{(\overline{A} \cdot \overline{\overline{B}}) + (\overline{CD} \cdot \overline{E})}$$

$$= \overline{(\overline{A}B) + (\overline{CD}\,\overline{E})}$$

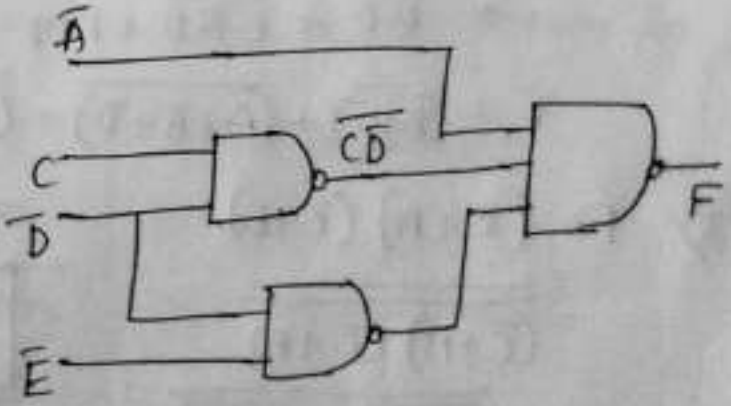
$$= \overline{\overline{AB}} \cdot \overline{\overline{CD} \cdot \overline{E}}$$



2) $F = A + C\overline{D} + \overline{D}\,\overline{E}$

$$= \overline{\overline{A + C\overline{D} + \overline{D}\,\overline{E}}}$$

$$= \overline{\overline{A} \cdot \overline{C\overline{D}} \cdot \overline{\overline{D}\,\overline{E}}}$$



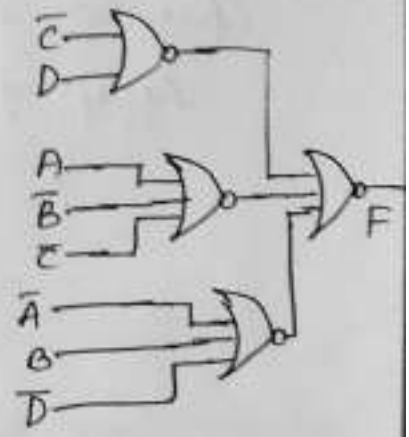
ii) Using NOR gates only:

To implement a Boolean function using NOR gates only, it is to be brought to the product of Sum (POS) form and then apply De-Morgan's theorem twice [Double complement Method].

Ex: $F = (\bar{C}+D)(A+\bar{B}+\bar{C})(\bar{A}+B+\bar{D})$

$$= \overline{\overline{(\bar{C}+D)(A+\bar{B}+\bar{C})(\bar{A}+B+\bar{D})}}$$

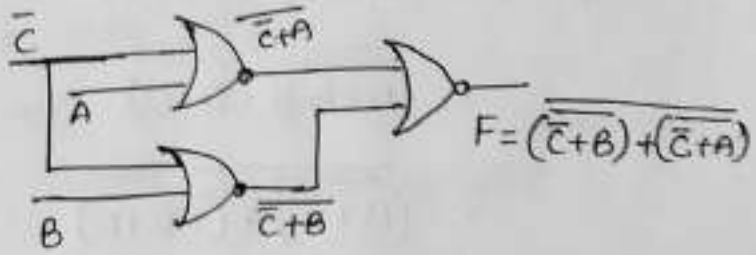
$$= \overline{\overline{(\bar{C}+D)} + \overline{(A+\bar{B}+\bar{C})} + \overline{(\bar{A}+B+\bar{D})}}$$



1) $F = (\bar{C}+A)(\bar{C}+B)$

$$= \overline{\overline{(\bar{C}+A)(\bar{C}+B)}}$$

$$F = \overline{\overline{(\bar{C}+A)} + \overline{(\bar{C}+B)}}$$



2) $F = \bar{B}\bar{D} + \bar{A}BD + \bar{A}CD$

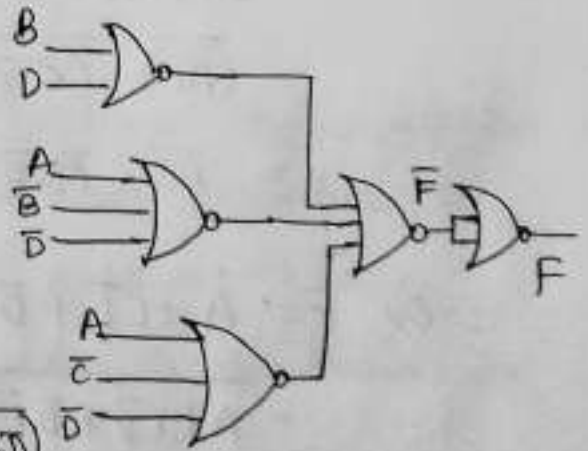
$$= \overline{\overline{\bar{B}\bar{D} + \bar{A}BD + \bar{A}CD}}$$

$$= \overline{\overline{\bar{B}\bar{D}} \cdot \overline{\bar{A}BD} \cdot \overline{\bar{A}CD}}$$

$$= \overline{(\overline{\bar{B}\bar{D}}) + (\overline{B\bar{A}D}) + (\overline{\bar{A}CD})}$$

$$= \overline{\bar{B}\bar{D}} + \overline{B\bar{A}D} + \overline{\bar{A}CD}$$

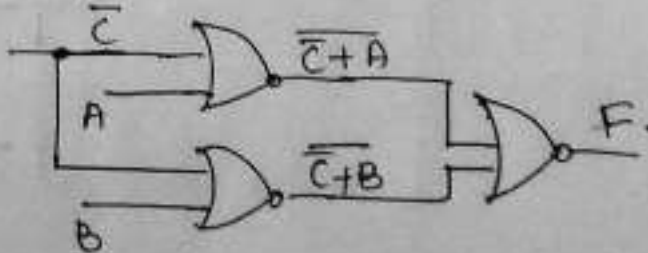
$$F = \overline{(B+D)} + \overline{(A+\bar{B}+\bar{D})} + \overline{(A+\bar{C}+\bar{D})}$$



3) $F = (\bar{C}+A)(\bar{C}+B)$

$$= \overline{\overline{(\bar{C}+A)(\bar{C}+B)}}$$

$$= \overline{(\overline{\bar{C}+A}) + (\overline{\bar{C}+B})}$$



ADDERS:

Computer perform various arithmetic operations. The most basic operations is the addition of two binary digits. The simple addition consists of four possible elementary operations, namely.

$0+0=0$

$0+1=1$

$1+0=1$

$1+1=10$

$$\begin{array}{r} {\scriptstyle 1}\ {\scriptstyle 1} \\ 1 \\ \hline 10 \leftarrow \text{Sum} \end{array}$$

↑ Carry.

* The first three operations produce a sum whose length is one-digit but when the last operation is performed, sum is two digits.
* The higher significant bit of this result is called a carry & lower significant bit is called Sum.

HALF ADDER

It is a Logic ckt which performs the addition of two bits & adds two binary numbers bit by bit giving the sum and possibly a carry.

The symbol for half adder is as shown in fig below.

A & B → i/p's

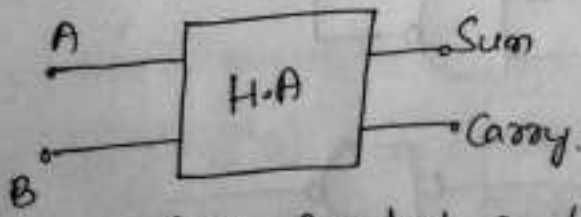


fig: Symbol of Half adder.

Truth-table:

A	B	S	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

From the truth table:

Sum = $\bar{A}B + A\bar{B}$.

Carry = AB.

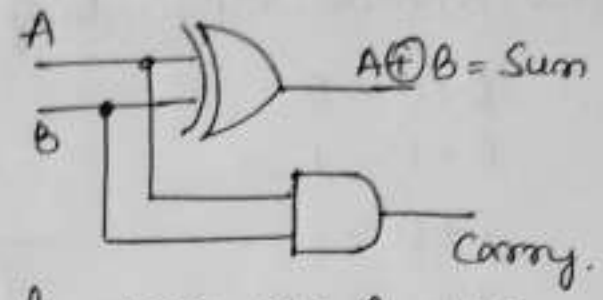
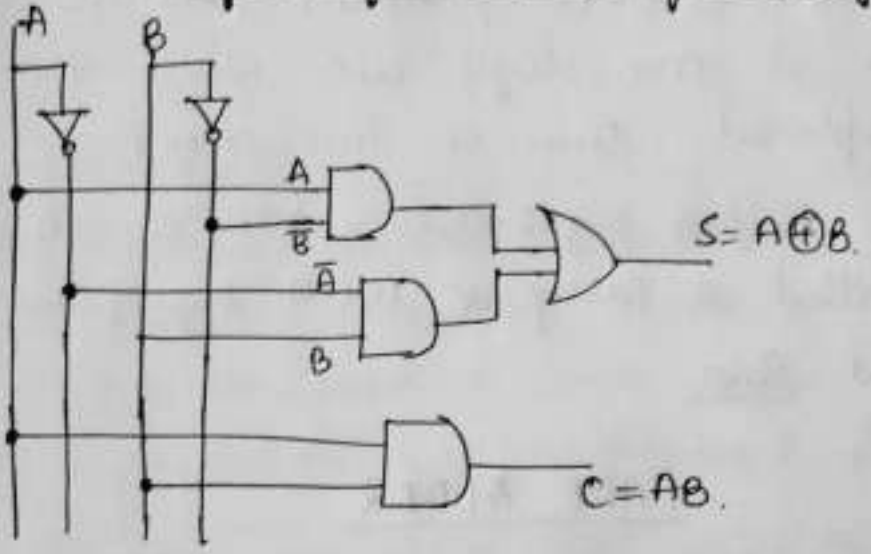
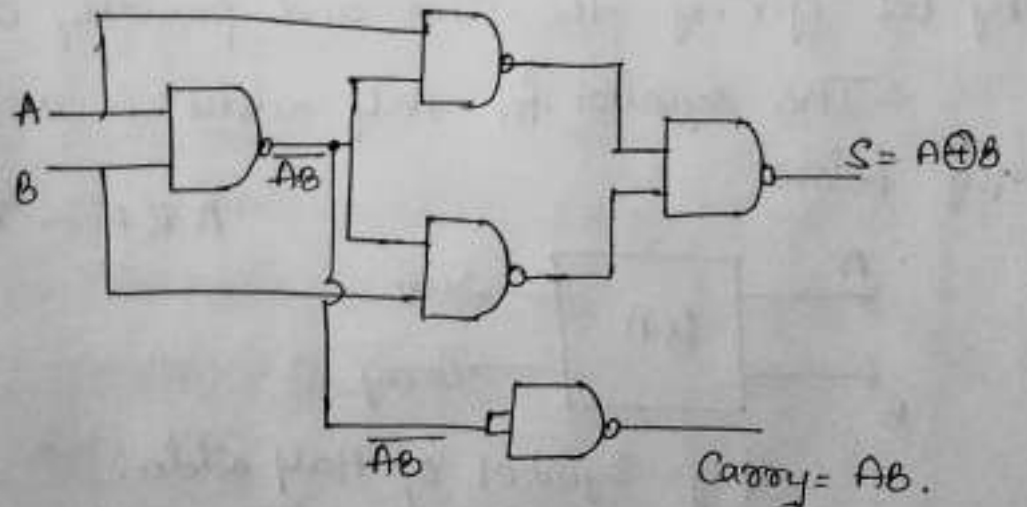


fig: Logic ckt for H.A.

Implementation of Half adder using basic gates



Realization of Half adder using only NAND Gates



Limitations of Half Adder

* In multidigit addition we have to add two bit along with the carry of previous digit addition So such addition requires addition of three bits. This is not possible with half adder.

Hence half adder are not used in practice.

FULL ADDER

In the full adder, three bits can be added at a time. The 3rd bit is a carry from the previous lower significant position. Thus Full adder is a combinational logic ckt. that performs the arithmetic sum of three i/p bits.

The three i/p bits are A, B, and C_{in}. and it has 2 outputs. Sum and Carry. The third i/p C_{in}, represents the carry from the previous lower significant bit. The symbol for Full adder is as shown in fig.

fig: Symbol for FA.

Truth Table.

A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

From the truth table:

$$Sum = \bar{A}B\bar{C_{in}} + \bar{A}B\bar{C_{in}} + A\bar{B}\bar{C_{in}} + ABC_{in}$$

$$= \bar{C_{in}}(\bar{A}B + A\bar{B}) + C_{in}[\bar{A}\bar{B} + AB]$$

$$= \bar{C_{in}}(A \oplus B) + C_{in}[A \odot B]$$

Let $A \oplus B = X$

$\therefore A \odot B = \bar{X}$

$= \bar{C}_{in} x + C_{in} \bar{x}$

$= C_{in} \oplus x.$

$\therefore Sum = C_{in} \oplus A \oplus B$

$C_{out} = \bar{A}BC_{in} + A\bar{B}C_{in} + AB\bar{C}_{in} + ABC_{in}$

$= \bar{A}BC_{in} + A\bar{B}C_{in} + AB[\bar{C}_{in} + C_{in}]$

$= \bar{A}BC_{in} + A\bar{B}C_{in} + AB.$

$= \bar{A}BC_{in} + A(\bar{B}C_{in} + B)$

$= \bar{A}BC_{in} + A(B + C_{in})$

$= \bar{A}BC_{in} + AB + AC_{in}$

$= B(\bar{A}C_{in} + A) + AC_{in}$

$= B(A + C_{in}) + AC_{in}$

$\boxed{C_{out} = AB + AC_{in} + BC_{in}}$

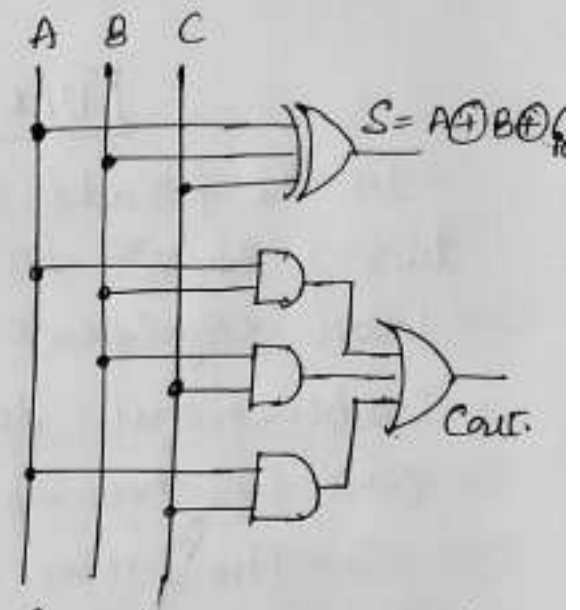


fig: logic ckt using Basic gates.

Full adder can also be implemented by using two half adders & one OR gate as shown in figure below. The Sum expression remains same but Cout expression can be simplified further

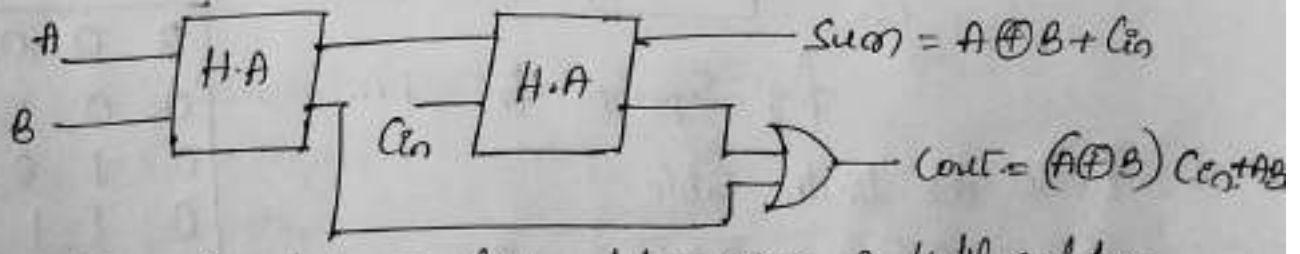


fig: Symbol of full adder using 2 Half adders.

$Sum = A \oplus C_{in} \oplus B.$

$C_{out} = \bar{A}BC_{in} + A\bar{B}C_{in} + AB\bar{C}_{in} + ABC_{in}$

$= AB[\bar{C}_{in} + C_{in}] + C_{in}[\bar{A}B + A\bar{B}]$

$= AB + C_{in}(A \oplus B).$

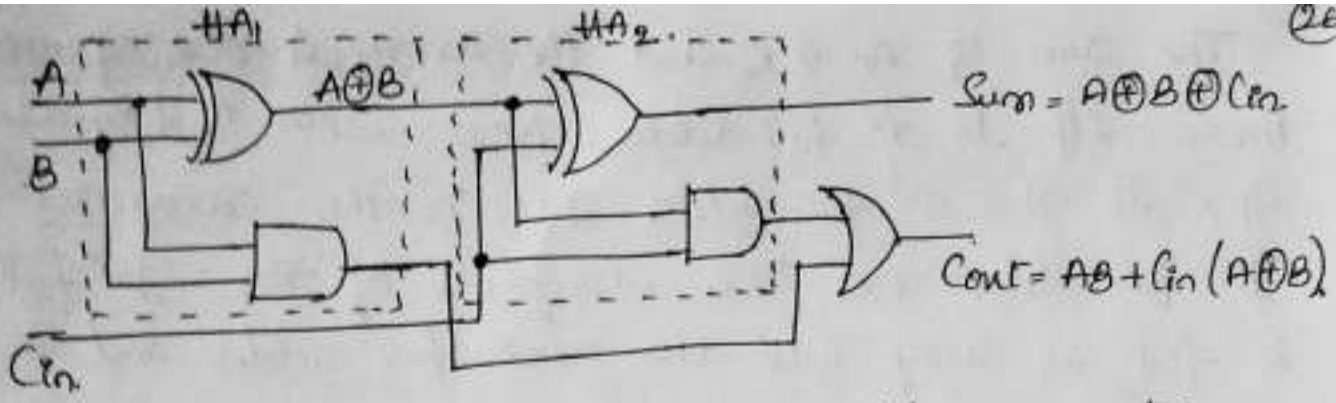


fig: Logic diagram of full adder using two Half Adders.

PARALLEL ADDER

We know that by using one full adder we can add two one bit & an i/p carry bit. The addition of multibit numbers can be accomplished by using several full adder.

The circuit which perform multibit addition simultaneously is called parallel Binary Adder. A N-bit parallel adder can be constructed using N- number of full adder circuits connected in parallel.

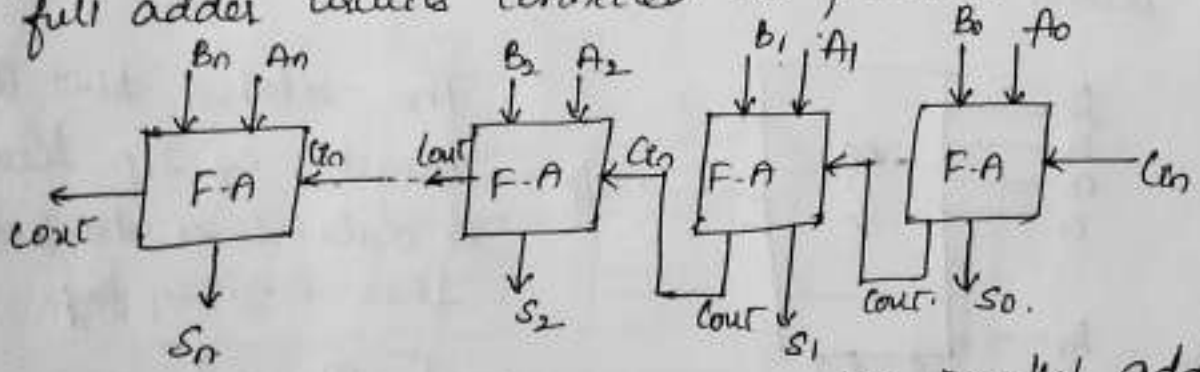


fig: Block diagram of n-bit parallel adder.

In the above figure, the carry o/p of each adder is connected to the carry i/p of the next- higher order adder.

It should be noted that either a half adder can be used for least significant position & the carry i/p of a full adder is made '0' because there is no carry into the least significant bit position.

The Sum of A_0 & B_0 and the carry is one of the three i/p to 1st full adder. Next with A_1 & B_1 are the i/p's to the 2nd full adder & C_{in} is the carryout of the 1st full adder i.e. The carryout of the 1st full adder is fed as carry into the next full adder and so on.

MULTIPLEXER [MUX].

Multiplexer is also called as MUX. It is a logic ckt that accepts several inputs and allows only one of them to get through the output at a time. It is also called as Data selector

The Select lines determines which input is connected to the output, and also increases the amount of data that can be sent over a network within a certain time. The Symbol for mux is as shown in figure below.

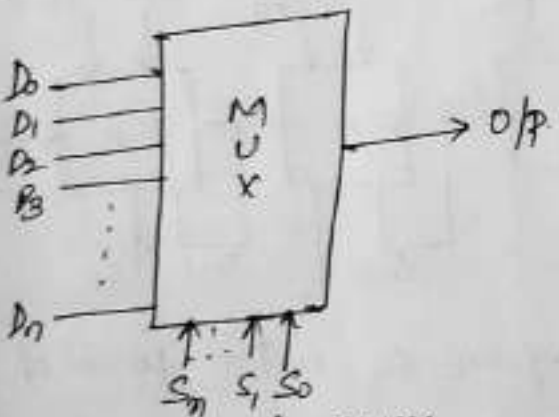


fig: Symbol for MUX.

The relation b/w the number of i/p lines & data lines to select lines is given by.

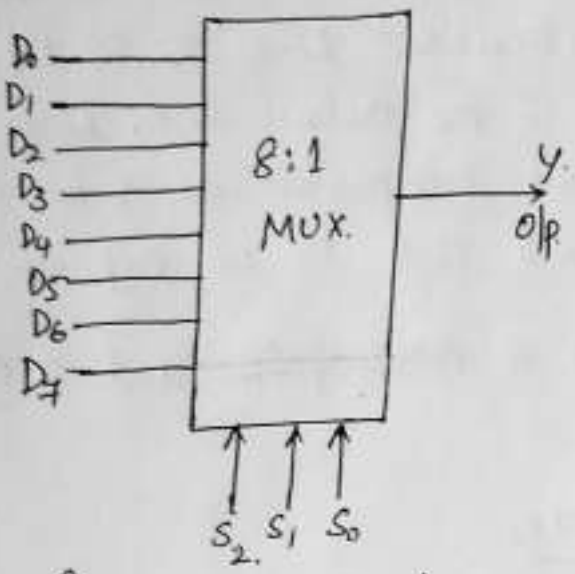
$$2^m = n$$

where m = no of select lines.
n = no of Data lines.

∴ For 8:1 MUX: $n = 8$. ∴ $2^m = 8$
$2^m = 2^3 \Rightarrow \boxed{m = 3}$.

for 4:1 MUX: $n = 4$ ∴ $2^m = 4$
$2^2 = 4 \Rightarrow \boxed{m = 2}$

Implementation of 8:1 MUX



Select lines			output
S_2	S_1	S_0	Y
0	0	0	D_0
0	0	1	D_1
0	1	0	D_2
0	1	1	D_3
1	0	0	D_4
1	0	1	D_5
1	1	0	D_6
1	1	1	D_7.

fig: 8:1 Multiplexer symbol

∴ From the truth table,

$$Y = \bar{S}_2\bar{S}_1\bar{S}_0 D_0 + \bar{S}_2\bar{S}_1 S_0 D_1 + \bar{S}_2 S_1 \bar{S}_0 D_2 + \bar{S}_2 S_1 S_0 D_3 + S_2\bar{S}_1\bar{S}_0 D_4 + S_2\bar{S}_1 S_0 D_5 + S_2 S_1 \bar{S}_0 D_6 + S_2 S_1 S_0 D_7.$$

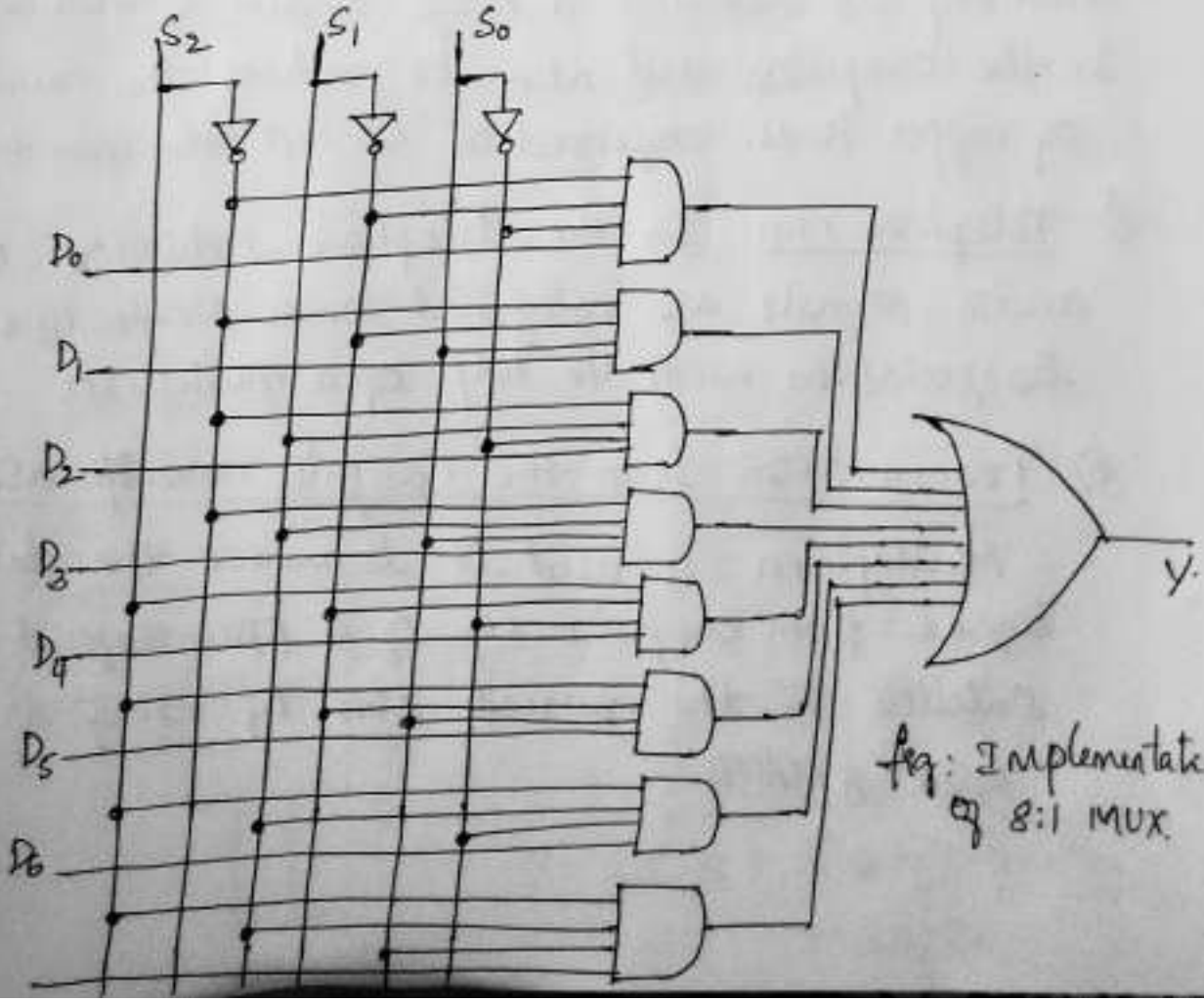


fig: Implementation of 8:1 MUX

The fig above shows the block diagram symbol and implementation of 8:1 MUX. which connects Eight 3 bit inputs to a common destination. Lines D_0 to D_7 are the Data input lines and Y is the output line. lines S_2, S_1, S_0 are the select lines. which interpreted as 3-bit binary choose one of the data line to be o/p on the Y.

8:1 MUX requires 8 AND gates and a OR gate and 3 select lines.

Advantages of Multiplexers.

1) Reduces the number of wires.
2) Reduces the circuit complexity and cost.

Applications of Multiplexers.

1) Computer memory: MUX are used in computer memory to maintain a huge amount of memory in the computers and also to reduce the number of copper lines. required to connect the memory.

2) Telephone nlw: In the telephone networks, multiple audio signals are integrated on a single line of transmission with the help of a multiplexer.

3) Transmission from the computer sln of a Satellite.

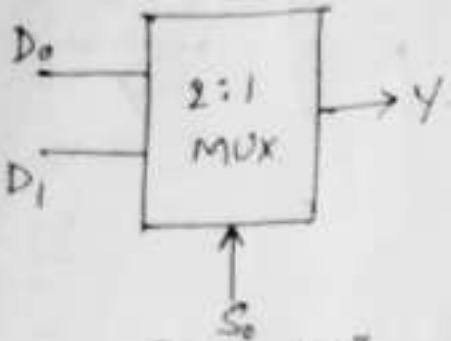
Multiplexer is used to transmit the data signals from computer sln of a spacecraft & a Satellite to the ground sln by using a GSM Satellite.

Ex ① Implement 2:1 MUX and Explain.

Given number of I/p's = 2. i.e $n = 2$.

∴ Number of select lines, $m = 1$.

The block diagram is,



Select line	o/p
S_0	Y
0	D_0
1	D_1

$\therefore Y = \bar{S_0} D_0 + S_0 D_1$

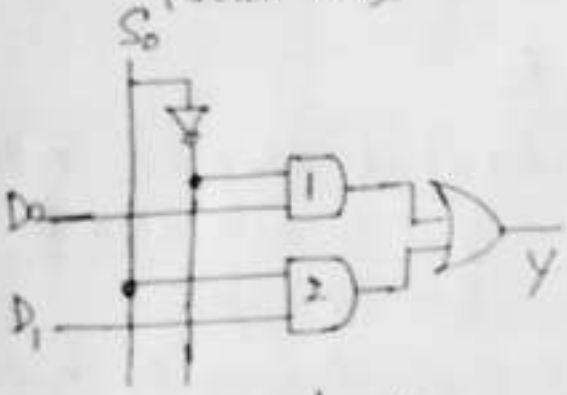


fig: Logic diagram.

When $S_0 = 0$. AND gate ① is activated & enabled and gate ② is disabled. $\therefore Y = D_0$.

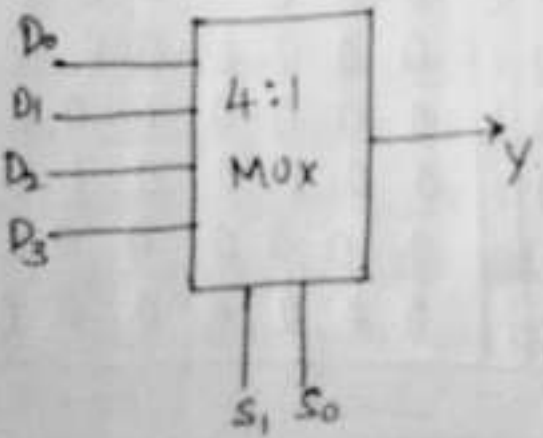
When $S_0 = 1$ AND gate ② is enabled and gate ① is disabled $\therefore Y = D_1$.

② Implement 4:1 MUX

Given number of I/p's = 4 i.e $n = 4$

Number of select lines $m = 2$.

The block diagram is



S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

$Y = \bar{S_1}\bar{S_0} D_0 + \bar{S_1} S_0 D_1 + S_1 \bar{S_0} D_2 + S_1 S_0 D_3$.

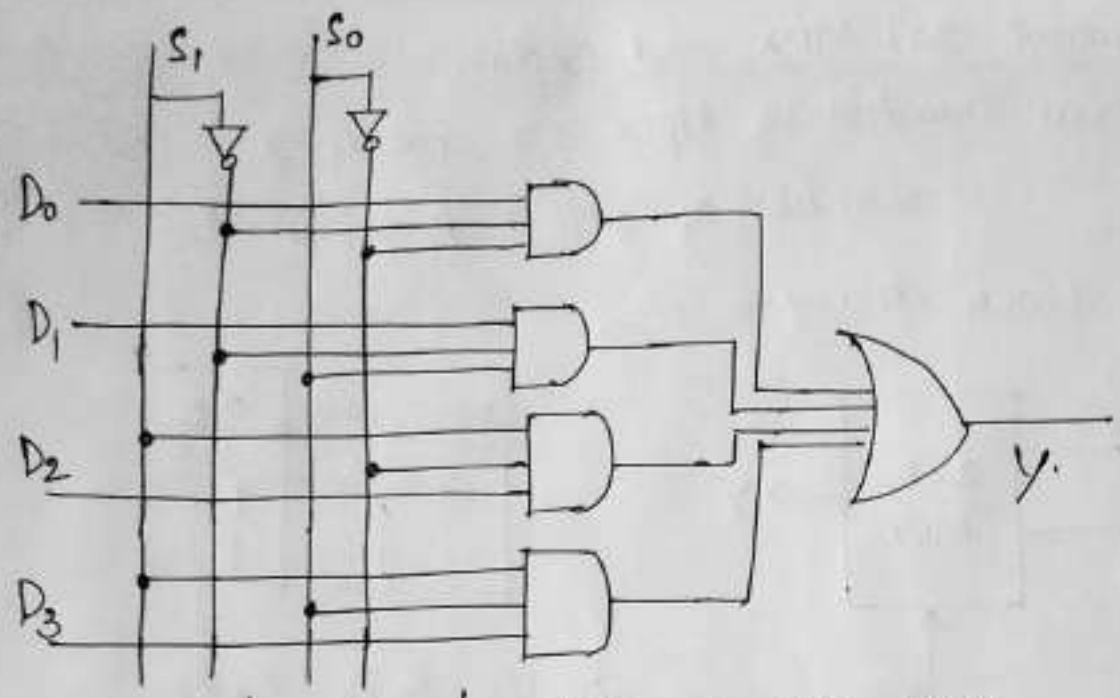
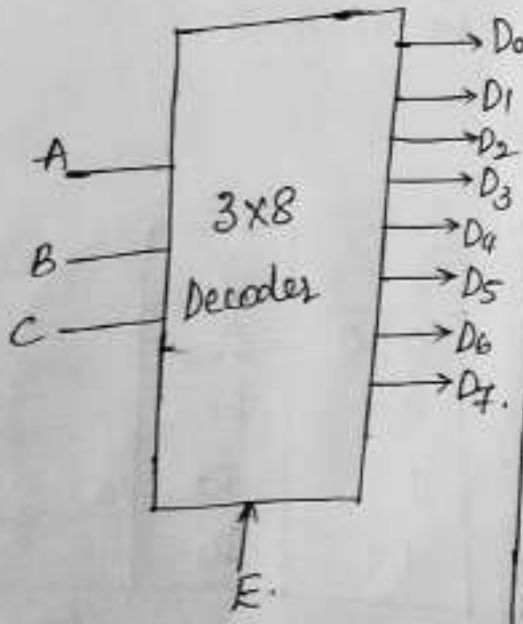


fig: Implementation of 4:1 MUX.

DECODER.

A Decoder is a combinational ckt that has n-inputs and 2^n outputs. only one output is activated for each one of the possible combination of input.

The Truth table and logic diagram of a 3x8 decoder is as shown in fig below.



E	A	B	C	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7.
0	X	X	X	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	0	1	0	0	0	0	0	0
1	0	1	0	0	0	1	0	0	0	0	0
1	0	1	1	0	0	0	1	0	0	0	0
1	1	0	0	0	0	0	0	1	0	0	0
1	1	0	1	0	0	0	0	0	1	0	0
1	1	1	0	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1

From the Truth table,

$D_0 = \bar{A}\bar{B}\bar{C}$ $D_3 = \bar{A}BC$ $D_6 = AB\bar{C}$

$D_1 = \bar{A}\bar{B}C$ $D_4 = A\bar{B}\bar{C}$ $D_7 = ABC$.

$D_2 = \bar{A}B\bar{C}$ $D_5 = A\bar{B}C$

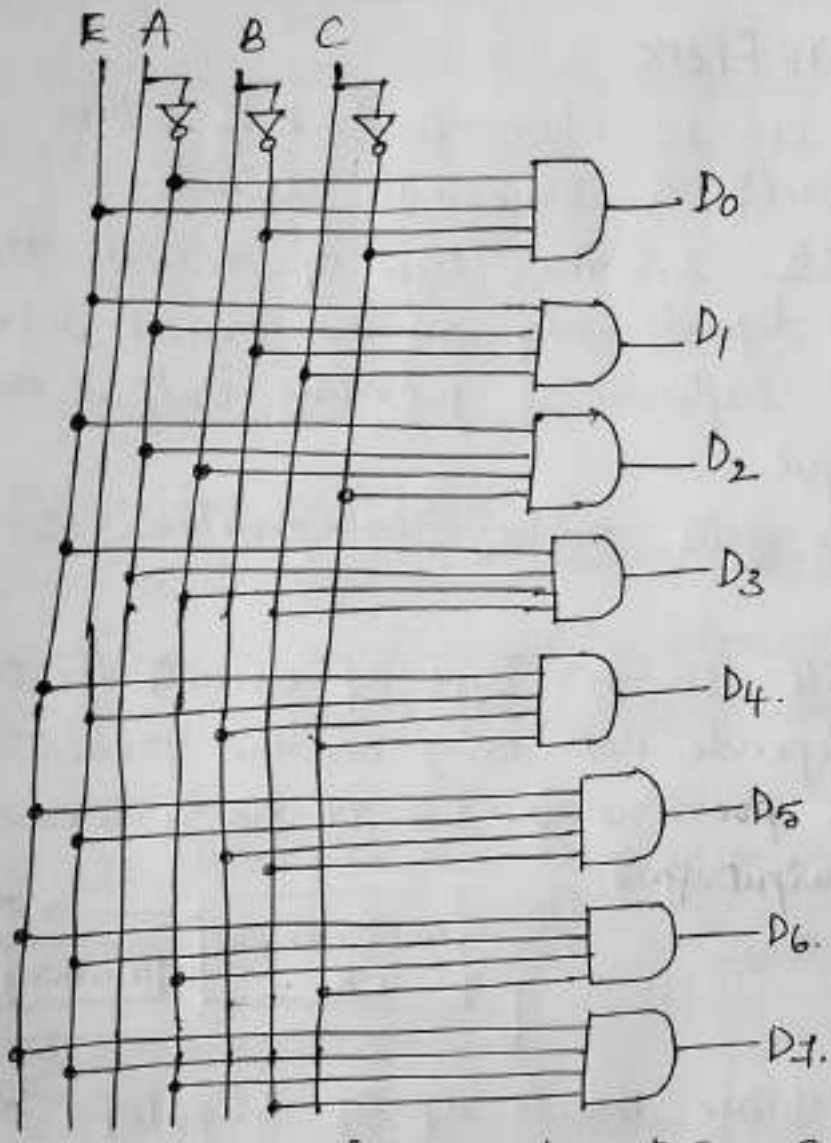


fig: Implementation of 3:8 Decoder

The circuit works only when Enable pin is high. A, B & C are different inputs and D_0 to D_7 are eight outputs. When enable input is 1 [E=1] and one of ip is active for given input. If i/p is A=1, B=1 and C=1 the output is 1 at D_7 rest of the outputs are zero. only one AND gate will be active for that particular combination of inputs. and Rest all of the AND gate will be disabled.

Applications:

Decoder are widely used in memory also of the computer, where they respond to the address code input from the central processor. to activate the memory storage location specified by address code.

FLIP FLOPS.

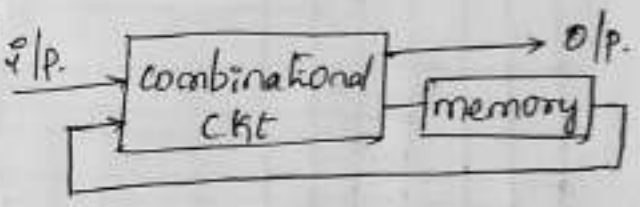
Digital circuits can be classified into either combinational circuits & Sequential circuits.

Combinational Circuits: In this type of circuits the o/p of the circuit depends only on the present input. And there is no influence of previous output on the present output.

ex: All the Basic gates. Adders. Comparators, MUX, Decoder

Sequential Circuits: In this type of circuits the o/p of the circuit depends not only on the present i/p but also on the previous o/p. i.e It has a memory to store the past outputs.

ex: Timers, counters, Registers.



Sequential circuits are made up of Flipflops & Latches.

Flipflop: Flipflop is a sequential ckt. and is a bistable element. which has one & more inputs and two o/p's and a clock input. It has a memory memory. Its output has two stable states i.e Logic 1 and Logic '0' hence it is called Bistable element.

Flipflop requires a clock signal to be applied at its i/p for operation.

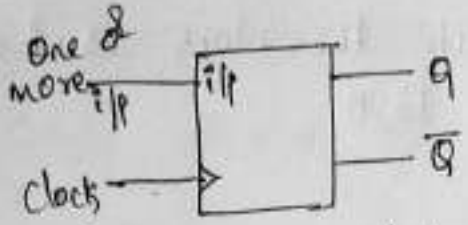


fig: Logic symbol of flipflop

Types of Flipflops:

1) SR Flipflop [Set-Reset flipflop].
2) JK flipflop [Jock Kilby flipflop]
3) D-Flipflop [Data flipflop]
4) T- Flipflop [Toggle flip flop].
5) Master slave flipflop.

Applications of Flipflops.

1) It can be used as a memory element
2) It can be used as delay element
3) It can be used as building blocks of counters & Registers.
4) In RAM [Random Access Memory]
5) For Frequency Division.

clock Signal:

clock signal is a square pulse with 50-1 duty cycle. The flipflop changes the o/p's either at the leading edge of the clock signal & falling edge of the clock signal.

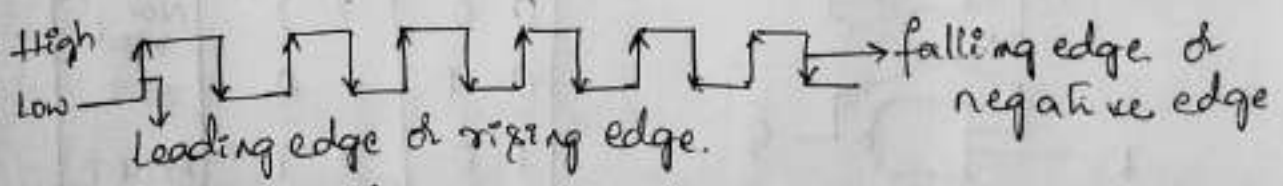


fig: clock signal.

Leading edge: The state at which the clock is changing from Low to High state i.e from 0 to 1

Falling edge: The state at which the clock is changing from high to low i.e from '1' to '0'

$$\text{Clock frequency} = \frac{1}{\text{Time period}}$$

SR LATCH

Latch is a building block of the flipflop. The simplest type of latch is SR latch. SR Latch can store two stable states. It has two inputs (SET) S & R (RESET) R. and 2 outputs. Q and $\bar{Q}$. The two outputs are complement to each other.

The figure below shows the block symbol of the logic symbol for SR latch. The SR latch can be easily implemented using NAND gates & NOR gates.

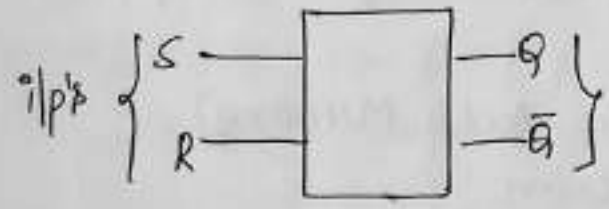
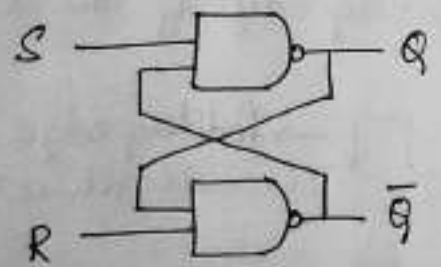


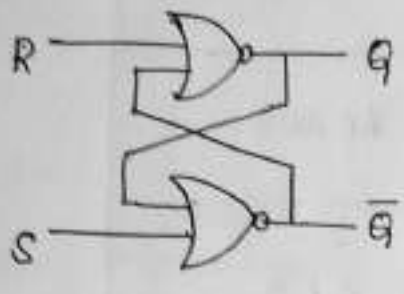
fig: logic symbol for SR Latch.

NAND Gate Latch: The NAND Latch is constructed using cross coupled NAND gates as shown in fig.



S	R	Q	$\bar{Q}$	State
0	0	?	?	Not used
0	1	1	0	SET
1	0	0	1	RESET
1	1	Q	$\bar{Q}$	No Change

NOR Gate Latch: The NOR gate Latch is constructed using cross coupled NOR gates as shown in fig.



S	R	Q	$\bar{Q}$	State
0	0	Q	$\bar{Q}$	No change
0	1	0	1	RESET
1	0	1	0	SET
1	1	?	?	Invalid.

Triggering methods for Flipflops

1) Enable 2) +ve edge trigger 3) -ve edge trigger.

Gated SR Flipflop:

Two inverters are connected with SR latch which gives SR flipflop as shown in figure. The gated SR flipflop is a modified form of a SR latch. i.e sensitive to inputs only when an enable input is active such flipflop is shown below.

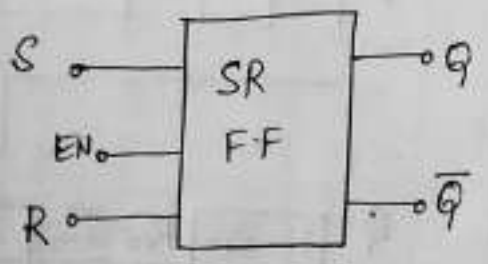


fig: Logic symbol

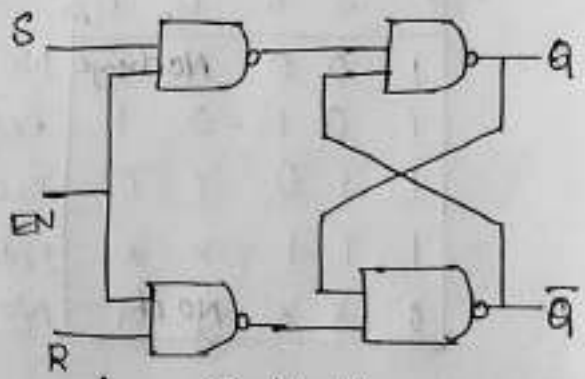


fig: SR flipflop with Enable

The circuit analysis and the truth table. The timing diagram for an gated SR flipflop is as shown below.

EN	S	R	present state Q_n	Q_{n+1}	state.
1	0	0	0	0	No change
1	0	0	1	1	
1	0	1	0	0	RESET
1	0	1	1	0	
1	1	0	0	1	SET
1	1	0	1	1	
1	1	1	0	x	Intermediate.
1	1	1	1	x	
0	x	x	0	0	No change.
0	x	x	1	1	

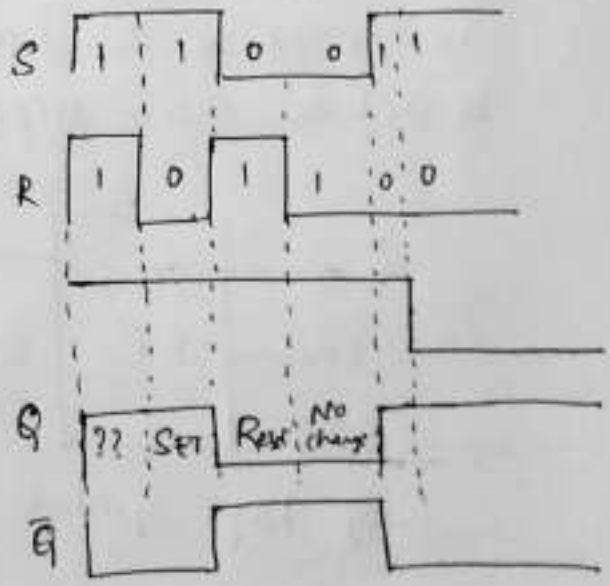
$Q_n \rightarrow$ present state [Assumption].

$Q_{n+1} \rightarrow$ Next state.

Truth table:

E	S	R	Q	$\bar{Q}$	
1	0	0	Q	$\bar{Q}$	No change.
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	x	x	Intermediate
0	x	x	Q	$\bar{Q}$	No change

Timing Diagram



Positive Edge triggered SR-Flipflop

In positive edge triggered flipflops the clock samples the input line at positive edge of the clock pulse. The state of the o/p of the flip flop is set & reset depending upon the state of input only at

positive edge of the clock. This state of the output remains for the one clock cycle. and the clock again samples the input line on the next positive edge of the clock.

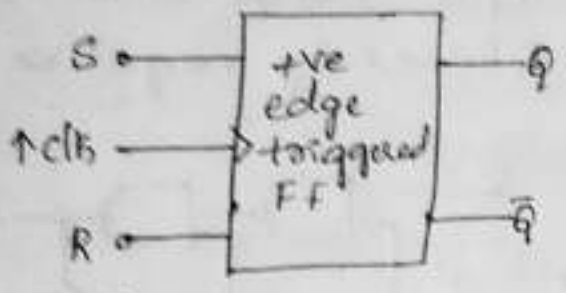


fig: Logic Symbol

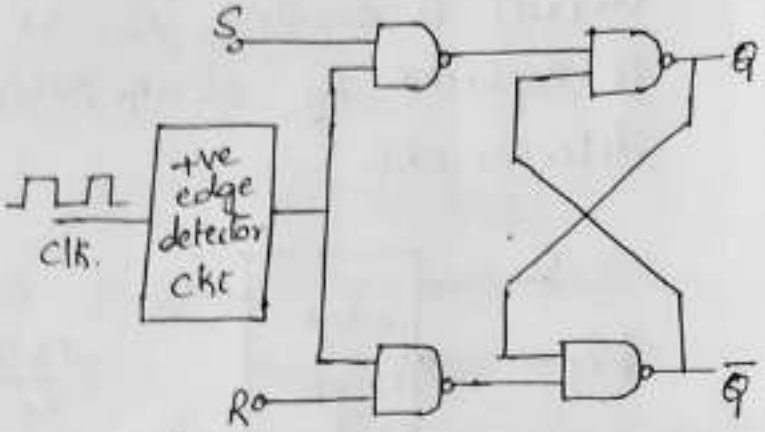


fig: Flip Flop using NAND.

The above figure shows the Logic symbol for clocked RS Flipflop and the ckt using NAND. The circuit is similar to gated SR flipflop except enable signal is replaced by clock pulse, followed positive edge detector ckt. The edge detector ckt is a differentiator. The circuit output responds to S & R inputs only at +ve edges of clock pulses.

CP	S	R	Q_n	Q_{n+1}	State
↑	0	0	0	0	No change
↑	0	0	1	1	
↑	0	1	0	0	RESET
↑	0	1	1	0	
↑	1	0	0	1	SET
↑	1	0	1	1	
↑	1	1	0	X	Intermediate
↑	1	1	1	X	
1	X	X	0	0	No change
0	X	X	1	1	

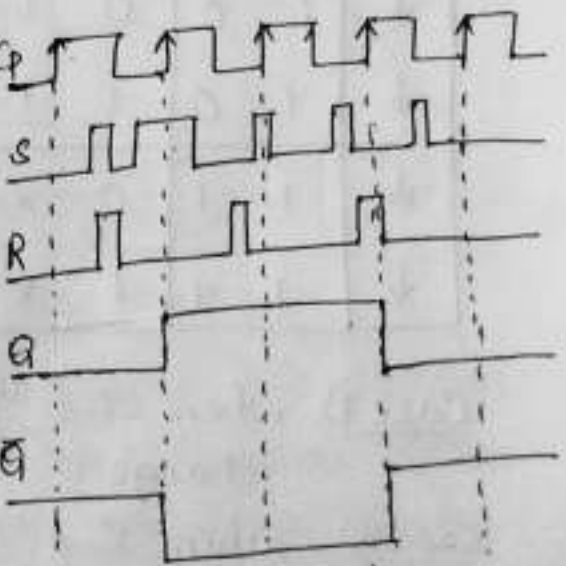


fig: Timing diagram

Negative Edge triggered SR Flipflop

The figure below shows the logic symbol and circuit for negative edge triggered SR flipflop. The circuit is similar to SR flipflop except enable signal is replaced by clock pulse. followed by negative edge detector ckt.

fig: Logic symbol

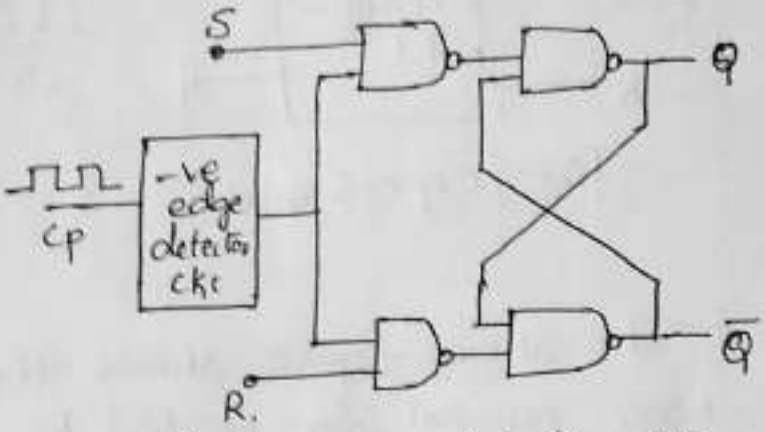
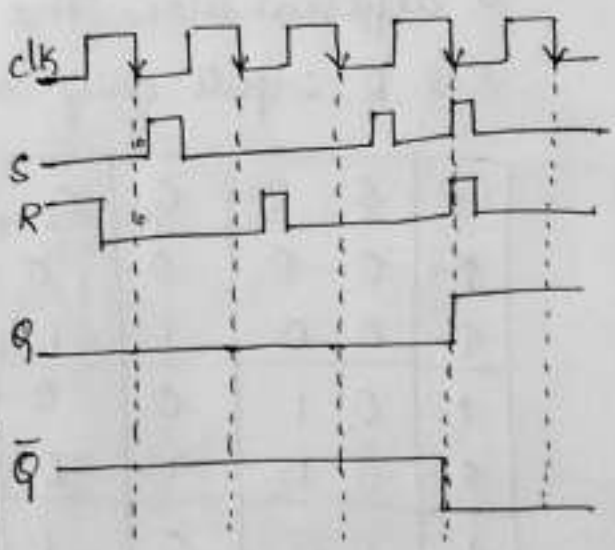


fig: ckt symbol for -ve edge triggered RS F·F.

Cp	S	R	Q_n	Q_{n+1}	State
↓	0	0	0	0	No change
↓	0	0	1	1	
↓	0	1	0	0	Reset
↓	0	1	1	0	
↓	1	0	0	1	Set
↓	1	0	1	1	
↓	1	1	0	x	Intermediate
↓	1	1	1	x	



Timing Diagram

Case 1) when S=0, R=1, Cp is applied the o/p will not change

Case 2) when S=0. R=1. Cp is applied the o/p $Q_{n+1}=0$.

Case 3) When S=1, R=0 cp is applied. The output state will be Reset state i.e $Q_{n+1} = 1$.

Case 4) When S=1, R=1 cp is applied. The output state is indeterminate & undefined.

J-K Flip Flop [Jack Kilby Flipflop]

The SR flipflop circuit suffers from basic switching problems. i.e for S=1 & R=1 the output will go to the indeterminate state. To overcome these fundamental design problem with the SR flipflop The JK flipflop was developed.

The JK flipflop was invented by Jack Kilby. The JK flipflops has three inputs J, K and clk. The ckt & symbol and the truth table is given below.

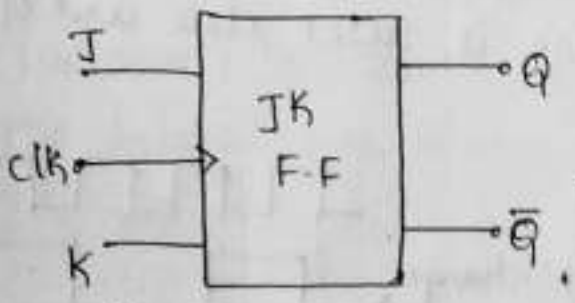


fig: Logic Symbol.

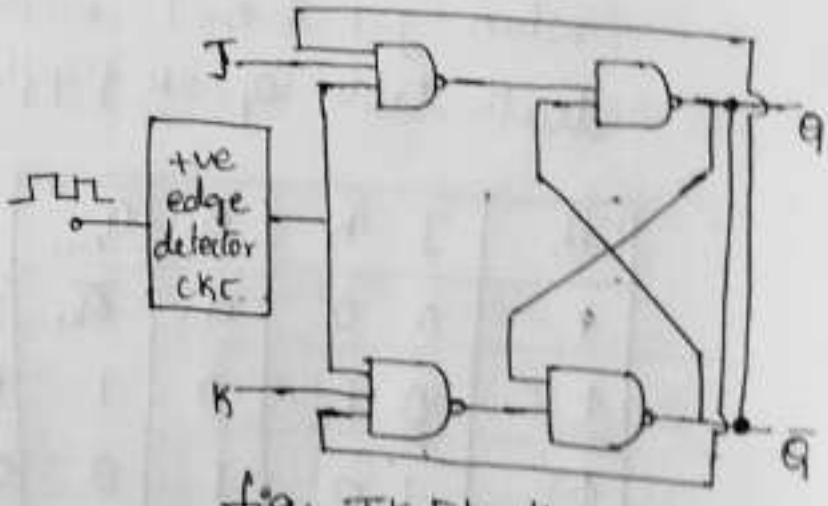


fig: JK Flipflop.

The JK flipflop is basically an SR flipflop with feedback which enables only one of its two input terminals. Either SET & RESET to be active at any one time thereby eliminating the invalid condition of the SR flipflop

When both J & K inputs are at logic '1' at the same time and the clock input is pulsed "High", the ckt will go toggle from SET state to RESET state & vice-versa. This results in JK.

1) $J = K = 0$: There is no change in the o/p.

2) $J = 1$: $K = 0$: when $J = 1$, $K = 0 \xrightarrow{\text{with } Q=0} S = 1$ & $R = 0$. According to the truth table of SR flipflop it is in set state and Q will be equal to 1.

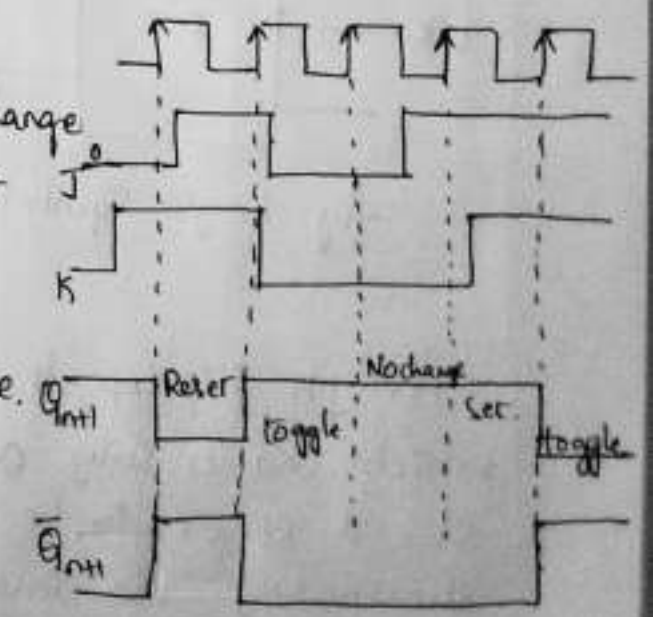
and with $Q = 1$, $S = 0$ & $R = 0$. Then there is nochange in o/p hence $Q = 1$ & $\bar{Q} = 0$.

3) $J = 0$: $K = 1 \Rightarrow S = 0$ & $R = 0$. The output will go to RESET state

4) $J = 1$; $K = 1 \Rightarrow$ When $J = 1$, $K = 1$ with $Q = 0$ $\bar{Q} = 1$. $S = 1$ and $R = 0$. From the truth table of SR flipflop is at SET state and output $Q = 1$

when $J = 1$ & $K = 1$ with $Q = 1$, $S = 0$ & $R = 1$ from the truth table of SR flipflop is reset state and $Q = 0$.

Clk	J	K	Q_{n+1}	$\bar{Q}_{n+1}$	
↑	0	0	Q_n	$\bar{Q}_n$	Nochange
↑	0	1	0	1	Reset
↑	1	0	1	0	Set
↑	1	1	$\bar{Q}_n$	Q_n	Toggle.



Race around condition:

The output toggles [i.e o/p changes from 0 to 1 or 1 to 0) in JK flipflop without any change in the i/p the output changes and value of Q is uncertain. This condition is called Race around condition. This exists when clock on period (tp) is higher than the propagation delay (Δt) by making $t_p < \Delta t$. we can overcome race around condition.

Master slave JK Flipflop

Master slave JK FF is a cascade of two SR flipflops with feedback from output of second to i/p of first. Master is a positive level triggered. But due to the presence of the inverter in the clock line the slave will respond to the negative level. Hence when clock=1 [positive level] the master is active and the slave is inactive, whereas when clock=0 (low level) the slave is active and master is inactive. The below fegure shows the symbol of Master slave JK flip flop.

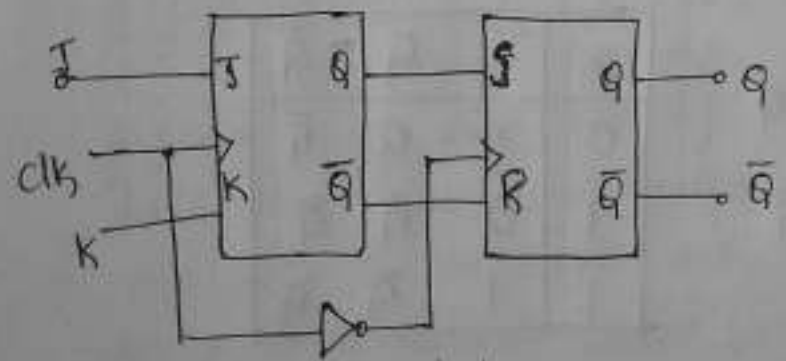


fig: Symbol.

Truth Table

clk	J	K	Q_{n+1}	$\bar{Q}_{n+1}$
1	0	0	Q_n	$\bar{Q}_n$
1	0	1	0	1
1	1	0	1	0
1	1	1	$\bar{Q}_n$	Q_n

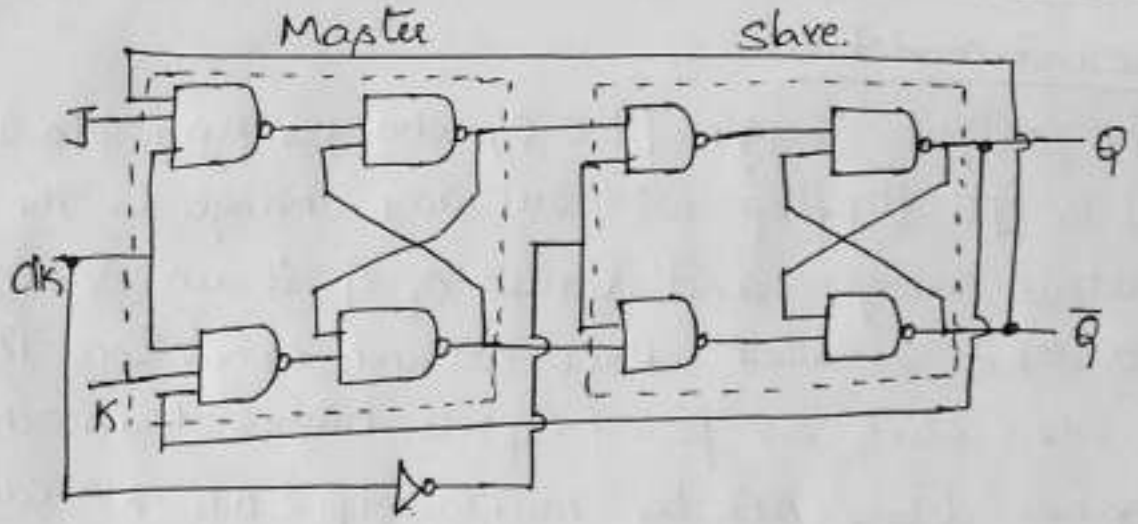
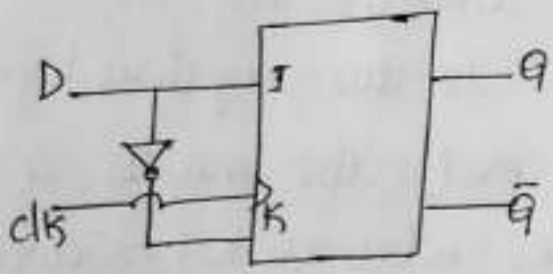


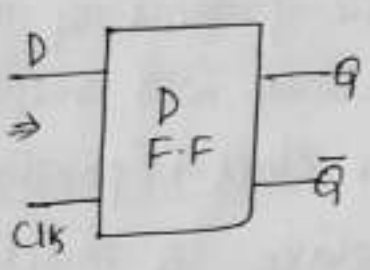
fig: Master slave JK flipflop.

Data Flipflop [D-flipflop].

This flipflop is obtained from JK flip flop by incorporating an inverter so that the K & J i/p becomes complement of each other. hence J=K=1 is eliminated.

Truth table

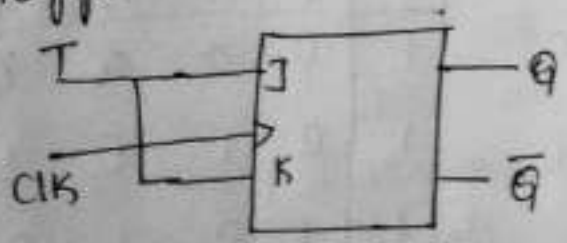




CLK	D	Q	$\bar{Q}$
0	X	Q	$\bar{Q}$
1	1	1	0
1	0	0	1

T-Flipflop [Toggle flipflop]

It is obtained from JK flipflop by connecting J & K inputs together. This type of FF acts as a Toggle switch.



CLK	T	Q	$\bar{Q}$
0	X	Q	$\bar{Q}$
1	0	Q	$\bar{Q}$
1	1	$\bar{Q}$	Q

Shift Registers

The shift register is also one of sequential logic circuit that can be used for the storage or the transfer of binary data. These are made up of flipflops which are connected in such a way that the output of the one flipflop could serve as the input to the other. depending on the type of the shift registers created.

These are commonly used inside the calculators & computers to store data such as two binary numbers. & to convert the data from either a serial to parallel & parallel to serial format.

The individual data latch that make up a single shift register are all driven by a common clock signal making them synchronous devices.

Shift Registers are of Four types

1) Serial In Serial Out [SISO]
2) Serial In Parallel Out [SIPO]
3) Parallel In Parallel Out [PIPO]
4) Parallel In Serial out [PISO].

Serial In Serial Out [SISO].

The input to this register is given in serial fashion i.e one bit after the other through a single data line and the output is collected serially. The data can be shifted only left or shifted right. Hence it is called Serial in Serial out shift register. A 4-bit SISO register consists of 4 flipflops as shown

in fig.

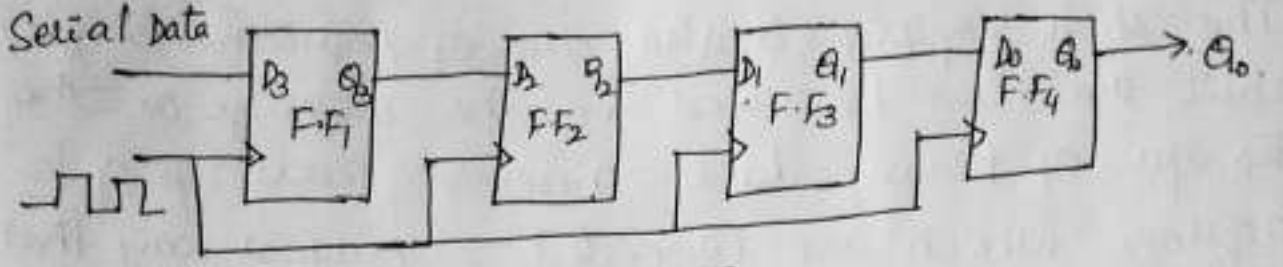


fig: 4 bit Shift Register.

In this, when clock signal is applied and the Serial data is given, only one bit is available at output at a time in the order of i/p data.

The use of SISO is to act as temporary data storage device. But the main use of a SISO is to act as a delay element.

Ex: let 4 bit data is 1011.

	clk	Data	Q_3	Q_2	Q_1	Q_0
(b)	Initially	1	0	0	0	0
	1	1	1	0	0	0
	2	0	1	1	0	0
	3	1	0	1	1	0
	4	1	1	0	1	1

Initially register will be cleared with $Q_3Q_2Q_1Q_0=0000$ when LSB is loaded at D with 1. This will gives the o/p only after the first clock pulse $Q_3=1$. Then load D=1, then after the second clk pulse $Q_3=1$ and $Q_2=1$. when D=0 then after third clock pulse $Q_3=0$, $Q_2=1$ and $Q_1=1$ when D=1, then after the 4th clock pulse $Q_3=1$ $Q_2=0$ $Q_1=1$ and $Q_0=1$.

2) Serial In parallel out: The register is loaded with serial data one bit by bit of bit at a time with

the stored data being available at o/p in parallel form.

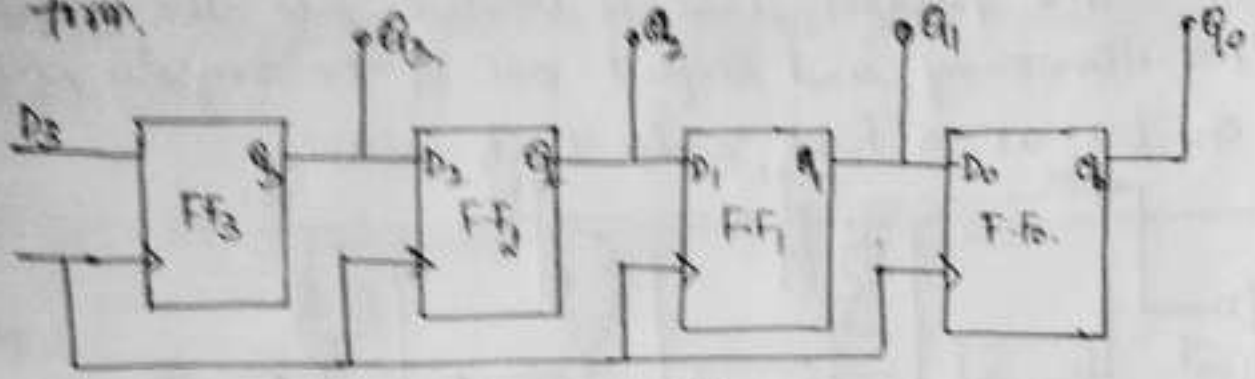


fig: Serial in parallel out.

Clk	D	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0	0
1	1	0	0	0	0
2	0	1	0	0	0
3	1	0	1	0	0
4	0	1	0	1	0

let D = 1010.

3) Parallel In parallel out [PIPO]

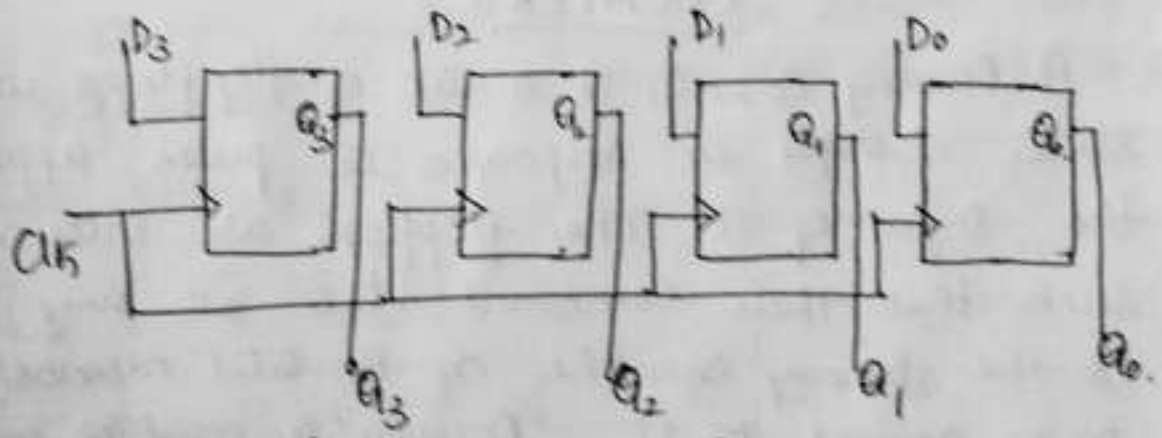


fig: PIPO Shift Register.

The data is loaded simultaneously into the Register and transferred together to their respective outputs by the same clock pulse.

4) Parallel In Serial out.

The parallel data is loaded into the register simultaneously and shifted out of the register serially one bit at a time under clock control.

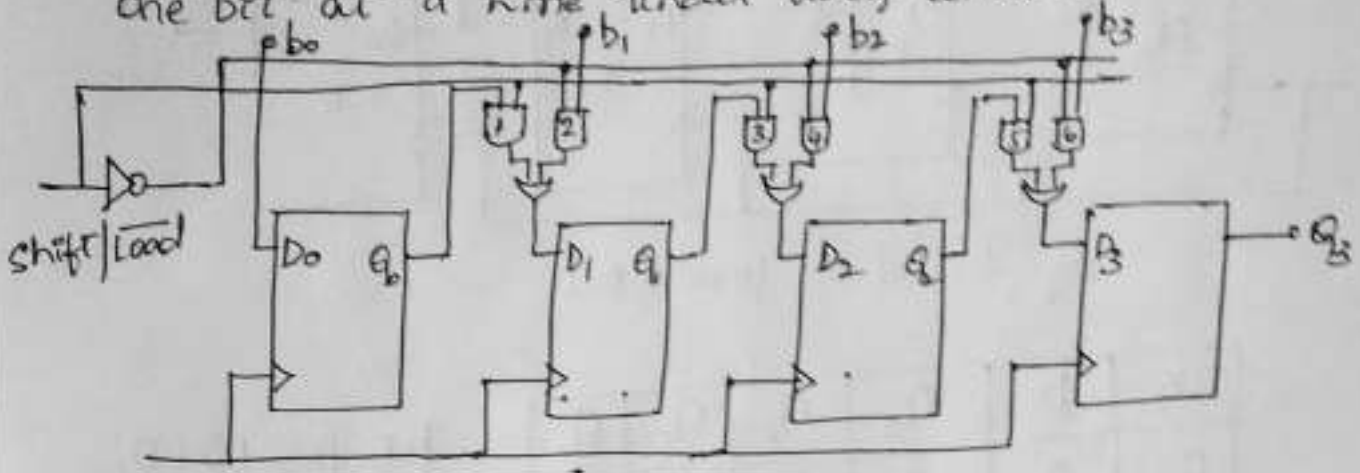


fig: PISO Shift Register

It has two modes one is load mode and shift mode. $\overline{Load}$ is a active low signal. Load = 0. Load will be activated and data will be loaded into Flipflops. when shift = 1, $\overline{Load}$ = 0. then it will shift operation to send data serially out.

COUNTERS

A Binary counter is a set of flip flops whose states changes in response to pulse applied at the input of it. The flipflops are inter connected such that their combined state at any time is the binary equalities of the total number of pulse applied to it. ∴ Counter is used to count pulses.

There are two types of counters

1) Asynchronous: In this, the o/p of the one flipflop will act as clk for the other. i.e there is no common clock. It is also called Ripple counter.

2) **Synchronous Counter:** There is a common clock blw all the Flipflops. All the flipflops start working with same clock.

3-bit Ripple Counter / Asynchronous Counter.

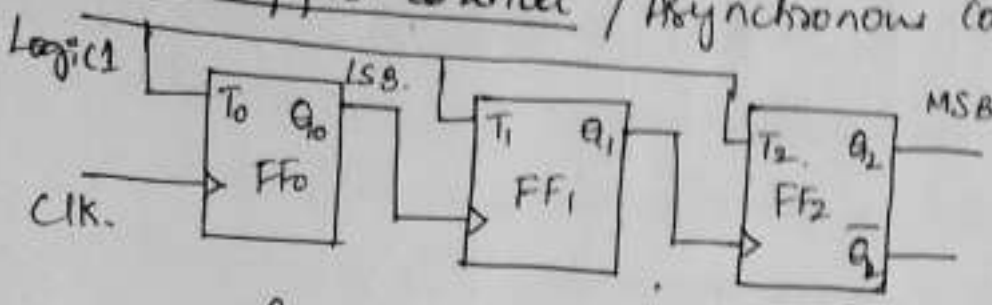
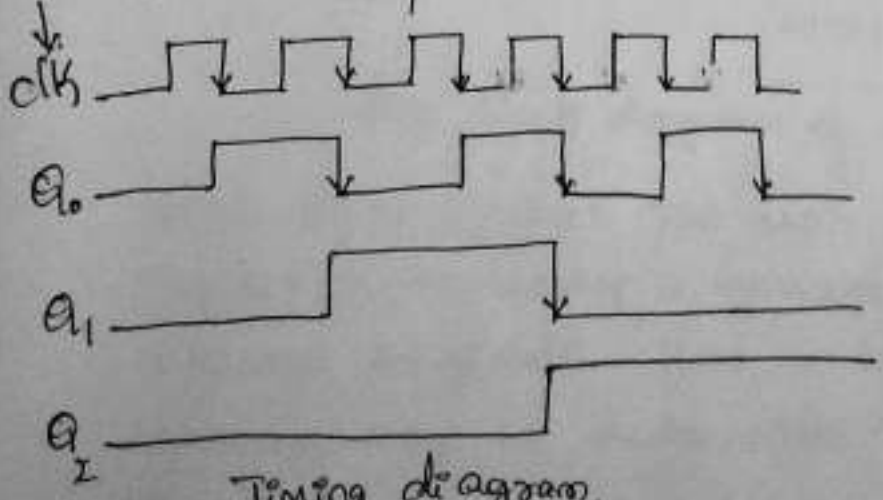


fig: 3-bit ripple counter [mod 8 counter]

The counter is initially is reset to $Q_0 Q_1 Q_2 = 000$. when the first clock pulse is applied FF_0 toggles at the negative edge of this pulse. ∴ Q_0 goes from Low to high. This becomes positive going edge at the i/p of FF_1 so FF_1 is not affected. Thus the state of the counter after first clock pulse is $Q_0 Q_1 Q_2 = 100$.

At the negative edge of the second clock pulse FF0 toggles so Q_0 change from High to Low. This process repeats.



Timing diagram.

CLK	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0

Communication Systems

Communication is the process of transferring information meaningfully from one point to another in an electronic mean. Meaningful information may be in the form of voice, text, picture or a combination of these.

A communication system involves the following stages.

1) Sorting, processing and storing of information.
2) Transmission with further processing and filtering of noise & unwanted information
3) Reception of information.

Elements of Communication Systems

A communication sim is an integration of various equipment needed for the process of communication. The figure below shows the block diagram of general communication system.

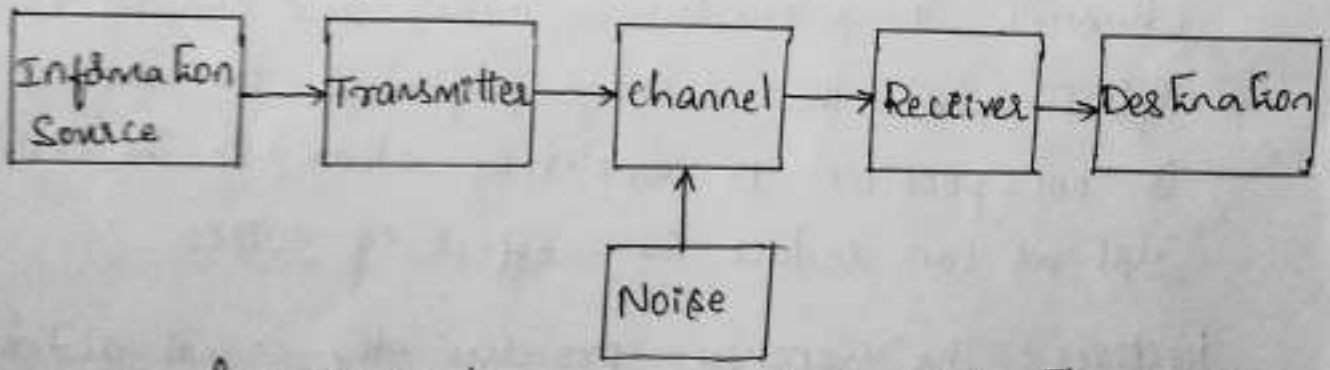


fig: Block diagram of a communication system.

Information Source: The main aim of the communication system is to convey a message called information. This message originates from an information source. The message may be Audio, video, text, image etc

Transmitter: It processes the input message signal to

make it suitable for sending it over the channel. This operation is termed as modulation. The transmitter consists of transducer and the modulator. Transducer is to convert the signal into electrical signal.

Channel: It is the physical medium & path that connects the transmitter and receiver. This may be pair of wires such as telephone wires or free space. There are 2 types of channels.

1) Wired channel: co-axial cable, optical fibre cable etc
2) Wireless channel: free space, microwave, wireless links etc

Wired channel is also called Line communication.
Wireless channel is also called Radio communication.

Noise: Noise is an unwanted signal that gets added to the message signal during transmission over the channel. It is random in nature and has its greatest effect when the message signal is the weakest. It is not possible to completely eliminate the noise just we can reduce the effect of noise.

Receiver: The receiver processes the signal and makes an estimate of the actual message that is transmitted It is a process called demodulation, which is the reverse of modulation and extraction of the information superimposed on the carrier wave. The reciever in addition to demodulation also performs amplification and filtering.

Modulation:

It is a process in which some characteristics & properties & parameters of high frequency sine wave called carrier wave is varied in accordance with the instantaneous value of the message signal called the modulating signal & baseband signal.

A sine wave carrier which is a high frequency signal, is represented as

$$v_c = V_C \sin(\omega_c t + \phi).$$

Where,

v_c = the instantaneous value of the carrier

V_C = the peak & the maximum amplitude of the carrier wave

ω_c = the angular frequency of the carrier

ϕ = the phase angle of the carrier

The characterics of carrier wave are amplitude, frequency, phase Accordingly we have three types of modulation.

1) Amplitude modulation
2) Freqeuncy modulation
3) phase modulation

Need for Modulation in Communication System

The direct transmission of the message signal such as voice, video & binary data, results in interference problem when transmission distance is too large i.e The low frequency signals can't be travel for long

distances. If we transmit for a longer distances they get attenuated. To carry out reliable long radio communication, it is neccesary to modulate signal because of the following reasons.

1) To reduce the height of Antenna

The minimum height of the antenna required for the efficient transmission is

$$h = \frac{\lambda}{4}$$

we know that $\lambda = \frac{c}{f} \because c = f\lambda$

$$\therefore \boxed{h = \frac{c}{4f}}$$

where, λ = wavelength
f = frequency of the signal
c = speed of electromagnetic wave $3\times10^8\ ms^{-1}$

ex: ① To transmit a signal of frequency, $f = 20kHz$.

$$h = \frac{3\times10^8}{4\times20\times10^3} = 3.75KM.$$

② To transmit a signal of frequency, $f = 20MHz$.

$$h = \frac{3\times10^8}{4\times20\times10^6} = 3.75m.$$

Here height of the antenna is inversely proportional to frequency of the signal. therefore the frequency can be changed by modulation hence the height of the antenna

2) To Avoid Mixing of Signals.

The frequency range of audio wave is blw 20Hz - 20KHz. If there are several stations operating

at same frequency range then different stations will be mixed up.

3) To increase the range of communication.

At low frequency, the radiation is very poor and signals gets highly attenuated. So message signals cannot be transmitted over a long distance hence modulation is used.

4) To allow multiplexing of signals.

The technique of transmitting more signals simultaneously on a single channel using a different frequency range by a process of modulation is known as frequency division multiplexing [FDM] ex: FM.

5) To allow adjustments in Bandwidth

The Bandwidth of the modulating signal can't be varried in the original signal because of noise. So, proper control of bandwidth is done in modulating signal

6) To improve the quality of Reception.

If the carrier frequency range is high then the signals are transmitted properly to recievers. The modulation techniques such as (FM/PCM) frequency modulation and pulse code modulation reduce the effect of noise to a great extent.